APPENDIX A

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

Nos. 2022-1465,
2022-1466, 2022-1467

ARBOR GLOBAL STRATEGIES, LLC, APPELLANT

v.

SAMSUNG ELECTRONICS CO., LTD., TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., APPELLEES

KATHERINE K. VIDAL, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE, INTERVENOR

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2020-01020, IPR2020-01021, IPR2020-01022

Nos. 2022-1549, 2022-1550,
2022-1551,2022-1552

ARBOR GLOBAL STRATEGIES, LLC, APPELLANT

v.

XILINX, INC., TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD., APPELLEES

KATHERINE K. VIDAL, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE, INTERVENOR

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2020-01567, IPR2020-01568, IPR2020-01570, IPR2020-01571

Decided: July 16, 2024

JUDGEMENT

DANIEL NOAH LERMAN, Kramer Levin Naftalis & Frankel LLP, Washington, DC, argued for appellant. Also represented by PAUL J. ANDRE, JAMES R. HANNAH, LISA KOBIALKA, Redwood Shores, CA, JEFFREY PRICE, New York, NY.

JOHN C. O'QUINN, Kirkland & Ellis LLP, Washington, DC, argued for appellees Samsung Electronics Co., Ltd., Taiwan Semiconductor Manufacturing Company, Ltd. Samsung Electronic Co., Ltd. also represented by WILLIAM H. BURGESS, CHRISTOPHER MIZZO; MEREDITH ZINANNI, Chicago, IL.

JAMES M. GLASS, Quinn Emanuel Urquhart & Sullivan, LLP, New York, NY, for appellee Taiwan Semiconductor Manufacturing Company, Ltd. Also represented by ERIC HUANG.

JEFFREY SHNEIDMAN, Fish & Richardson P.C., Boston, MA, argued for appellee Xilinx, Inc. Also

represented by KENNETH WAYNE DARBY, DAVID M. HOFFMAN, Austin, TX; JOHN A. DRAGSETH, Minneapolis, MN.

DANA KAERSVANG, Civil Division, United States Department of Justice, Washington, DC, argued for intervenor. Also represented by BRIAN M. BOYNTON, JOSHUA MARC SALZMAN; MICHAEL S. FORMAN, FARHEENA YASMEEN RASHEED, MICHAEL TYLER, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA.

THIS CAUSE having been heard and considered, it is

ORDERED and ADJUDGED:

PER CURIAM (HUGHES, LINN, and STARK, *Circuit Judges*).

AFFIRMED. *See* Fed. Cir. R. 36.

ENTERED BY ORDER OF THE COURT

/s/ Jarrett B. Perlow
Jarrett B. Perlow
Clerk of Court

July 16, 2024
Date

APPENDIX B

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case IPR2020-01021
Patent 7,282,951 B2

SAMSUNG ELECTRONICS, CO., LTD., PETITIONER,

v.

ARBOR GLOBAL STRATEGIES, LLC, PATENT OWNER.

Entered: Dec. 2, 2020

DECISION

Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1, 4, 5, 8, 10, and 13–15 (the "challenged claims") of U.S. Patent No. 7,282,951 B2 (Ex. 1001, "the '951 patent"). Petitioner filed a Declaration of Dr. Stanley Shanfield (Ex. 1002) with its Petition. Arbor Global Strategies LLC ("Patent Owner"), filed a Preliminary Response (Paper 7, "Prelim. Resp."). Pursuant to the Board's Order

(Paper 8), the parties filed additional briefing to address the Board's discretionary authority to deny a petition based on a parallel district court proceeding under 35 U.S.C. § 314(b). Paper 9 ("Pet. Prelim. Reply"); Paper 10 ("PO Prelim. Sur-reply").

The Board has authority to determine whether to institute an *inter partes* review ("IPR"). *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), we may not authorize an *inter partes* review unless the information in the Petition and the Preliminary Response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we institute an *inter partes* review as to the challenged claims of the '951 patent on all grounds of unpatentability presented.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. Pet. 74. Patent Owner identifies Arbor Global Strategies LLC. Paper 5, 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC* v. *Samsung Electronics Co., Ltd. et al.*, 2:19-cv-00333-JRG-RSP (E.D.Tex.) (filed October 11, 2019) ("District Court" or "District Court Action") as a related infringement action involving the '951 and two related patents, U.S. Patent No. RE42,035 E and U.S. Patent No. 6,781,226 B2, which contain the same specification as the '951 patent. *See* Pet. 74; Paper 5.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in the two related patents, respectively IPR2020-01020 and IPR2020-01022.

C. *The '951 patent*

The '951 patent describes a stack of integrated circuit ("IC") die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '951 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." *Id.*

Figure 4 follows:

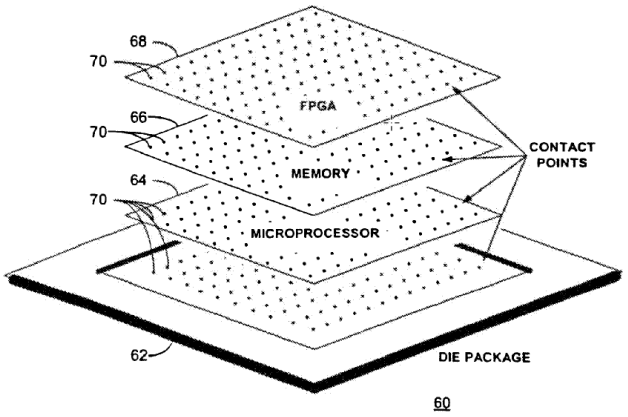

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64,

interconnected using metal and contact holes 70. Ex. 1001, 4:61–5:7.

The '951 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:26–41. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See id.* A "reconfigurable processor" provides a known benefit of flexibly providing the specific functional units required by an application after manufacture. *See id.*

D. *Illustrative Claims 1 and 10*

The Petition challenges independent claims 1, 5, and 10, and claims 4, 8, and 13–15, dependent respectively therefrom. Claims 1 and 10 illustrate the challenged claims at issue:

> 1. A processor module comprising:
>
> [1.1] at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and
>
> [1.2] at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element [1.3] wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements and [1.4] wherein said second integrated circuit includes a

memory array functional to accelerate external memory references to the processing element.

Ex. 1001, 7:58–8:4 (information added by Board to conform to Petitioner's nomenclature); *see* Pet. 23–30 (addressing claim 1).

10. A processor module comprising:

at least a first integrated circuit functional element including a programmable array;

at least a second integrated circuit functional element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit functional element; and

at least a third integrated circuit functional element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit functional elements respectively wherein said memory is functional to accelerate external memory references to said programmable array.

Ex. 1001, 8:42–55.

E. *The Asserted Grounds*

Petitioner challenges claims 1, 4, 5, 8, 10, 13–15 of the '951 patent on the following grounds (Pet. 2):

Claims Challenged	35 U.S.C. §	References
1, 4, 5, 8, 10, 13–15	103[1]	Koyanagi,[2] Alexander[3]
1, 4, 5, 8, 10, 13–15	103	Bertin, Cooke[4]

II. DISCRETION TO DENY INSTITUTION UNDER § 314(a)

Patent Owner argues that "[t]he Board should deny the Petition because institution of this proceeding under § 314(a) because it would not be consistent with the objective of the AIA to 'provide an effective and efficient alternative to district court litigation.'" Prelim. Resp. 3 (quoting *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential) ("*NHK*").

In *NHK*, the Board declined to institute *inter partes* review, in part, because "under the facts and circumstances," a review "would be an inefficient use of Board resources," given the status of a parallel

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[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of institution, the '951 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

[2] M. Koyanagi et al., "Future System-on-silicon LSI Chips," IEEE Micro, Vol. 18, Issue 4, July/August 1998. Ex. 1007.

[3] M.J. Alexander et al., "Three-dimensional Field-programmable Gate Arrays," Proceedings of Eighth International Application Specific Integrated Circuits Conference, September 18–22, 1995. Ex. 1006.

[4] Cooke, US 5,970,254, issued Oct. 19, 1999. Ex. 1008.

district court proceeding between the same parties. *NHK*, Paper 8 at 20. The Board considered the following factors in *NHK*: (1) based on the district court's schedule, the district court's trial would conclude "before any trial on the [p]etition concludes"; and (2) the petitioner relied on the "same prior art and arguments" as its district court invalidity contentions, so the Board would "analyze the same issues" as the district court. *Id.* at 19–20.

As with other non-dispositive factors considered for institution under § 314(a), the Board weighs an early trial date as part of a "balanced assessment of all relevant circumstances in the case, including the merits." Patent Trial and Appeal Board Consolidated Trial Practice Guide 58 & n.2 (Nov. 2019), https://www.uspto.gov/TrialPracticeGuideConsolidated ("CTPG") (discussing follow-on petitions and parallel proceedings, citing *NHK* and *General Plastic Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017) (precedential)); *see Abbott Vascular, Inc. v. FlexStent, LLC*, IPR2019-00882, Paper 11 at 31 (PTAB Oct. 7, 2019) (declining to adopt a bright-line rule that an early trial date alone requires denial in every case).

Non-dispositive factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (Order analyzing *NHK* issues) (precedential) ("*Fintiv*"). Overlap among these factors often exists and some facts may be relevant to more than one factor. *See id.* Therefore, in evaluating the factors, the Board holistically views whether denying

or instituting review best serves the efficiency and integrity of the system. *See* CTPG at 58 (quoting 35 U.S.C. § 316(b)); *Fintiv*, Paper 11 at 6.

The precedential *Fintiv* order lists the following factors for consideration "when the patent owner raises an argument for discretionary denial under *NHK* due to an earlier trial date": 1) whether a stay exists or is likely to be granted if a proceeding is instituted; 2) proximity of the court's trial date to the Board's projected statutory deadline; 3) investment in the parallel proceeding by the court and parties; 4) overlap between issues raised in the petition and in the parallel proceeding; 5) whether the petitioner and the defendant in the parallel proceeding are the same party; and 6) other circumstances that impact the Board's exercise of discretion, including the merits. *See Fintiv*, Paper 11 at 5–16.

1. *Factor 1–Likelihood of Stay*

Patent Owner notes that the District Court denied Petitioner's motion to stay the District Court Action. Prelim. Resp. 4 (citing Ex. 2001 (motion to stay)); Ex. 2002 (denial)). Patent Owner contends that a stay "is highly unlikely" (*id.*) because the District Court informed that parties that Petitioner "may need to show that the Board is likely to invalidate every asserted claim—a showing that may require more than just pointing to a successful petition" (*id.* (quoting Ex. 2002, 6)). Patent Owner also argues that the District Court informed the parties that "Petitioner would only be permitted to refile the Motion 'if the Board institutes on all three Samsung petitions for *inter partes* review.'" *Id.* at 4 (quoting Ex. 2002, 5).

Analyzing the motion to stay, the District Court noted that the burden to show that a stay is appropriate had not been met "most importantly" because the Petitioner could not show that we had granted review on the Petitioner's three petitions for *inter partes* review. Ex. 2002, 3. The District Court noted that in *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018), the Supreme Court prohibited the Board's prior "partial institution" practice wherein "the Board would institute on a claim-by-claim basis, determining whether a particular claim had a reasonable likelihood of being invalidated." Ex. 2002, 5–6. The District Court then reasoned that "[s]ince the PTAB can no longer partially institute IPR proceedings, institution decisions may not be as useful as they were in the past for providing an indication of whether all [challenged] claims would be found unpatentable."

The Board herein determines that Petitioner has shown a reasonable likelihood of prevailing on all of the challenged claims. The dependent claims recite well-known circuitry or structure, including a memory array, a programmable memory array reconfigurable as a processor, an additional stacked integrated circuit element, and/or additional distributed contact points. *See* dependent claims 4, 8, and 13–15.

Because the Board institutes on all three petitions and Petitioner sets forth a strong showing of unpatentability on the challenged claims here, as discussed further below, and in the two other concurrent decisions to institute (IPR2020–01020, Paper 11; IPR2020-1022, Paper 11), the record indicates that, although Petitioner's motion for a stay was denied, the District Court is likely to allow

Petitioner to refile a motion for a stay and may grant it under the circumstances presented here. *See* Ex. 2002, 5–6. Accordingly, *Fintiv* factor 1 weighs slightly in favor of not exercising our discretion to deny institution.

2. *Factor 2–Trial Date Versus FWD Due Date*

Patent Owner contends that "[t]his parallel proceeding has been pending for nearly a year. During that time, the court set a case schedule, and trial is set to begin April 5, 2021, ***eight months before*** a Final Written Decision would be expected to issue." Prelim. Resp. 5.

When a district court's trial date will occur before the projected statutory deadline, the Board generally weighs this factor in favor of exercising authority to deny institution under § 314(a). *Fintiv*, Paper 11 at 9.

The fact that the District Court is likely to allow Petitioner to refile a motion for stay and may grant a stay creates uncertainty as to whether the trial actually will start on the presently scheduled date, and diminishes the extent to which this factor weighs in favor of exercising discretion to deny institution. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 9–10 (June 16, 2020) (informative) ("[B]ecause of the number of times the parties have jointly moved for and the district court agreed to extend the scheduling order dates . . . and the uncertainty that continues to surround the scheduled trial date, we find that this factor weighs marginally in favor of not exercising discretion to deny institution under 35 U.S.C. § 314(a)").

Given that the District Court's currently scheduled trial date falls roughly eight months prior to the projected statutory deadline for a final written decision, but accounting for the uncertainty due to a possible stay as to whether the trial actually will start on the currently scheduled date, *Fintiv* factor 2 weighs moderately in favor of exercising our discretion to deny institution.

3. *Factor 3–Investment in Proceedings*

Patent Owner contends "by the time the Board is due to issue its institution decision in this case, claim construction and fact discovery will have been completed." Prelim. Resp. 6 (citing Ex. 2003, 3). According to Patent Owner,

> [t]he parties have also already filed their Joint Claim Construction and Prehearing Statement. Ex. 2005. Claim Construction briefing and the Markman Hearing will be completed by November 10, 2020. Ex. 2003. Fact discovery closes shortly thereafter—on November 16, 2020. *Id*. Expert discovery is expected to close on December 21, 2020, which is roughly two weeks after the Board is due to issue its institution decision in this case. *Id*. Accordingly, even if the Board finds that one or more of the grounds asserted in this Petition raises a reasonable likelihood that a claim is unpatentable, the parties will have already concluded expert discovery before a single post- institution brief is filed in this case.

Prelim. Resp. 7.

The District Court's scheduling order generally supports Patent Owner's timeline. *See* Ex. 2003. After

the parties completed the supplementary briefing, the District Court issued a first amended docket control order, which moves the close of fact discovery to December 7, 2020, and the close of expert discovery to January 5, 2021. *See* Ex. 3002, 2. According further to Patent Owner, "[p]ursuant to that [original] Order and the Court's Patent Rules, Patent Owner served its preliminary infringement contentions, Petitioner served its invalidity contentions, and Patent Owner served corrected infringement contentions." Prelim. Resp. 7 (citing Ex. 2003).

The Board considers the overlap of investment prior to the institution decision. The record shows that the parties and the District Court invested some resources in the parallel district court litigation albeit with respect to the three related patents noted (*supra* § I.B) with some portion of the work relevant to patent validity of the '951 patent. For example, Petitioner argues and the District Court docket control order indicates that Petitioner served its invalidity contentions on May 4, 2020, about two months after Patent Owner served its infringement contentions on March 9, 2020. Ex. 2003, 4; Pet. 73. The docket control order also lists August 25, 2020 and September 8, 2020 respectively as the dates for filing amended pleadings and a response to the amended pleadings. *See* Ex. 2003. The parties do not inform the Board if the amended pleadings listed on the District Court's order correspond to the date Patent Owner "served corrected infringement contentions." *See* Prelim. Resp. 7. In any event, Petitioner filed the instant Petition on May 29, 2020—about 3.5 weeks after it served its initial invalidity contentions on May 4,

2020, the due date ordered by the District Court. *See* Ex. 2003.

Also, according to Patent Owner, "Patent Owner filed its Complaint for infringement on October 22 [sic], 2019.[5] Ex. 2004. Then, on February 6, 2020, Petitioner filed a Motion to Dismiss, which the Court denied on April 20, 2020. *See* Ex. 2002. Following a hearing on March 23, 2020, the court entered a Docket Control Order. Ex. 2003." Prelim. Resp. 6. Therefore, assuming a service date of sometime between October 11–22, 2019 (*see supra* note 5), Petitioner filed the instant Petition on May 29, 2020—over 4 months prior to the statutory time bar date (one year after date of service) under § 315(b). Furthermore, according to Patent Owner's timeline, Petitioner filed the Petition a little over 5 weeks after the District Court ruled on Petitioner's motion to dismiss. *See* Prelim. Resp. 6.

Petitioner's timing as outlined above mitigates this *Fintiv* factor. If a petitioner, "faced with the prospect of a looming trial date, waits until the district court trial has progressed significantly before filing a petition," that decision "may impose unfair costs to a patent owner." *Fintiv*, Paper 11 at On the other hand, "[i]f the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution." *Id.*

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[5] According to the District Court, Patent Owner filed the complaint on October 11, 2019. Ex. 2002, 1. The parties do not indicate the date of service of the complaint.

As discussed further in the next section, Petitioner's stipulation (Ex. 1025) minimizes the overlap or investment relative to the grounds in the IPR versus the invalidity challenges in the District Court Action. *See* Pet. Prelim. Reply 3 ("[B]ecause of Petitioner's stipulation, [the District Court] will not need to consider invalidity arguments based on the instituted grounds or grounds relying on the same primary reference as in the instituted grounds if the IPR is instituted."). Even though the Markman hearing already occurred (*see* Ex. 3002; Prelim. Resp. 7), the claim construction standard in the two proceedings is the same.

Considering the above-noted facts, including the time invested by the parties and the District Court, the extent to which the investment in the District Court Action relates to the issues of patent validity we would consider, and the timing of the filing of the Petition, this factor weighs slightly in favor of exercising our discretion to deny institution.

4. *Factor 4–Overlap of Issues*

This factor evaluates "concerns of inefficiency and the possibility of conflicting decisions" when substantially identical prior art is submitted in both the district court and the *inter partes* review proceedings. *Fintiv*, Paper 11 at 12.

Patent Owner argues that "the issues raised herein . . . overlap entirely with the art and issues raised the [D]istrict [C]ourt proceeding," so that "[t]his factor weighs very heavily in favor of discretionary denial." Prelim. Resp. 8 (citing Ex. 2006 (claim charts involving Koyanagi, Cooke and Bertin)). Petitioner responds it stipulated "that if the Board

institutes 'one or more of the IPR petitions on the grounds presented,' then Petitioner 'will not pursue those same instituted grounds or grounds based on the same primary reference' in the related district court litigation." Pet. Prelim. Reply 1 (quoting Ex. 1025 (stipulation)) (emphasis omitted).

Citing estoppel concerns under 35 U.S.C. § 315(e)(1), Patent Owner responds that "[a] meaningful stipulation in this case would have included not only the grounds and references actually raised in its Petition, but also all grounds that reasonably could have been raised." PO Prelim. Sur-reply 1 (citing *Sand Revolution*, Paper 24 at 12 n.5). Patent Owner adds that "[f]urthermore, Factor 4 concerns 'overlap between **issues raised** in the petition and in the parallel proceeding.'" *Id.* at 2 (quoting *Fintiv, Inc.*, Paper 11 at 6) (emphasis by Patent Owner).

Notwithstanding Patent Owner's arguments, Petitioner's stipulation here is broader than the stipulation in *Sand Revolution*, which states "if the IPR is instituted, Petitioner will not pursue the same grounds in the district court litigation." *Compare* Ex. 1025, 1–3, *with Sand Revolution*, Paper 24 at 11–12.[6] Like in *Sand Revolution*, Petitioner's stipulation here "mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as

[6] The stipulation here is broader than the stipulation in *Sand Revolution*, because although both stipulations preclude pursuing the "same grounds" in the *inter partes* reviews as the grounds employed in their respective district court trials, the stipulation here also precludes any "grounds based on the same primary reference" employed in the District Court.

well as concerns of potentially conflicting decisions." *Sand Revolution*, Paper 24 at 12.

In addition, the precedential *Fintiv* decision characterizes the precedential *NHK* decision as follows:

> In *NHK*, the patent owner argued the Board should deny institution under 35 U.S.C. § 314(a) because institution of a trial at the PTAB would be an inefficient use of Board resources in light of the "advanced state" of the parallel district court litigation *in which the petitioner had raised the same invalidity challenges*.

Fintiv, Paper 11 at 2 (quoting *NHK*, Paper 8 at 20) (emphasis added). And in *NHK*, in addition to relying on the advanced state of the district court trial to deny institution, the Board stated that in "[t]he district court proceeding, . . . Petitioner asserts *the same prior art and arguments*." *Id.* (emphasis added). The Board then reasoned "[i]nstitution of an inter partes review *under these circumstances* would not be consistent with 'an objective of the AIA . . . to provide an effective and efficient alternative to district court litigation.'" *Id.* (quoting *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, Case IPR2016-01357, Paper 19 at 16–17 (Sept. 6, 2017) (precedential as to § II.B.4.i) (emphasis added)).

Accordingly, *Fintiv* factor 4 weighs moderately in favor of not exercising our discretion to deny institution.

5. *Factor 5–Identity of Parties*

The District Court Action and the trial here involve the same parties. *See* Prelim. Resp. 8. "If a

petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact *against exercising discretion* to deny institution under *NHK*." *Fintiv*, Paper 11 at 13–14 (emphasis added).[7]

Accordingly, *Fintiv* factor 5 weighs slightly in favor of exercising our discretion to deny institution.

6. *Factor 6–Other Circumstances*

This final *Fintiv* factor represents a catch-all for any *other* relevant circumstances. Whether to exercise discretion to deny institution under § 314(a) involves "a balanced assessment of all relevant circumstances in the case, including the merits." CTPG 58.

Considering the parties' arguments in deciding the merits of the Petition and the Preliminary Response, Petitioner presents a strong showing on the merits here. In summary, on this preliminary record, Petitioner presents a strong showing stacking dies together with multiple contacts extending through the dies to connect circuits on the dies including processor, memory, FGPA circuits would have been obvious. *See infra* Section III.D–E; Pet. 11–71. In other words, Petitioner shows that the challenged claims largely involve a "combination of familiar

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[7] At least one Board member observed that *Fintiv* "says nothing about situations in which the petitioner is the same as, or is related to, the district court defendant." *Cisco Sys., Inc. v. Ramot at Tel Aviv Univ. Ltd.*, IPR2020-00122, Paper 15 at 10 (PTAB May 15, 2020) (APJ Crumbley, dissenting). According to the dissent in *Cisco*, if "the factor weighs in favor of denial if the parties are the same," this could "tip the scales against a petitioner merely for being a defendant in the district court." *Id.* at 11. This "would seem to be contrary to the goal of providing district court litigants an alternative venue to resolve questions of patentability." *Id.*

elements according to known methods . . . yield[ing] predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) ("The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results."). These predictable results include better performance in terms of speed, bandwidth, compactness, and power dissipation. *See infra* Section III.D–E; Pet. 11–71.

In addition, an IPR trial here avoids potentially complicated and overlapping jury issues of three related patents and allows the panel to focus on multiple issues in depth that involve not only the '951 patent, but also to consider related issues in the other two proceedings that may present a conflict with findings here. Therefore, this *inter partes* trial will provide the parties with an in-depth analysis of the '951 patent, providing a full record that will enhance the integrity of the patent system.

Accordingly, factor 6 weighs moderately in favor of not exercising our discretion to deny institution.

7. *Conclusion on § 314(a) Discretionary Denial*

Under *Fintiv*, the Board takes "a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Fintiv*, Paper 11 at 6. As discussed above, factor 2 weighs moderately and factors 3 and 5 weigh slightly in favor of exercising our discretion to deny institution. But factor 1 weighs slightly and factors 4 and 6 weigh moderately in favor of not exercising our discretion to deny institution.

Under a holistic analysis and under the particular circumstances of this case, the interests of

efficiency and integrity of the patent system tilt toward not invoking our discretionary authority under § 314(a) to deny institution of the Petition.

III. ANALYSIS

Petitioner challenges claims 1, 4, 5, 8, 10, and 13–15 as obvious based on the grounds listed above. Patent Owner disagrees.

A. *Legal Standards*

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR*, 550 U.S. at 406. Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. *Level of Ordinary Skill in the Art*

Relying on the testimony of Dr. Shanfield, Petitioner contends that

> [a] person of ordinary skill in the art ("POSITA") at the time of the alleged invention would have been a person having a Master's degree in

> Electrical Engineering, Computer Engineering, or Physics with three to five years of industry experience in integrated circuit design, layout, packaging or fabrication. Ex. 1002 ¶¶ 53–56. A greater level of experience in the relevant field may compensate for less education, and vice versa.

Pet. 10.

Patent Owner does not present a proposed level of ordinary skill. For purposes of this Decision on Institution, we adopt Petitioner's proposed level of ordinary skill in the art, which comports with the teachings of the '951 patent and the asserted prior art.

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

The parties' arguments raise a claim construction issue regarding "a memory array functional to accelerate external memory," "said memory array is *functional* to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array" as recited respectively in claims 1, 5, and 10. Neither party provides an explicit construction.

Addressing claim 1, Petitioner contends that the full scope of the "functional to accelerate external memory references to the processing element" claim requirement ('claimed acceleration') is unclear because neither the claims nor the specification describes a baseline from which to measure the claimed acceleration." Pet. 28. Petitioner contends that "the specification attributes the claimed acceleration to the stacking of an FPGA die and a memory die, whereby a wide configuration data port interconnects the stacked memory die and the FPGA using contact points distributed throughout the dies." *Id.* (citing Ex. 1001, 2:65–3:2 ("the FPGA module may employ stacking techniques to combine it with a memory die for the purpose of accelerating external memory references as well as to expand its on chip block memory"), 2:33–46).

Patent Owner alleges that Petitioner relies on a "require[d] . . . feature of a 'wide configuration data port' disclosed in the . . . '951 [p]atent [specification]." Prelim. Resp. 18 (citing Pet. 28). However, Patent Owner does not argue the claims require a wide configuration data port. *See* Prelim. Resp. 18 ("To the extent that the Board agrees with Petitioner that this claim element requires a wide configuration data port,

Koyanagi in view of Alexander does not teach a 'wide configuration data port,' let alone a wide configuration data port.").

Moreover, Patent Owner otherwise acknowledges that Petitioner does not rely on a wide configuration data port: "Petitioner alleges that Koyanagi's disclosure of 'the large number of contact points distributed throughout the dies form vertical interconnections that 'enable large data bandwidth in vertical data transfer' and thus 'accelerate' external memory references to the FPGA processing element.'" Prelim. Resp. 17 (quoting Pet. 29–30). However, Patent Owner contends that "the claims require a memory array—not a large number of contact points—that is functional to accelerate external memory references to the processing element." *Id.* at 18.

Other than a large number of contact points, Patent Owner does not draw attention to a disclosure in the '951 patent that describes certain structure of "a memory array . . . that is functional to accelerate external memory references to the processing element." *See* Prelim. Resp. 18.

As Patent Owner argues, Petitioner relies on the '951 patent's description of "interconnect[ing] the stacked memory die and the FPGA using contact points distributed throughout the dies" as providing the "functional to accelerate external memory references to the processing element" limitation. *See* Pet. 29–30 (quoting Ex. 1001, 2:41–46 (contacts are placed "throughout the total area of the various die rather than just around their periphery" to obtain "many more connections between the die"); citing Ex. 1001, 2:65–3:2; Ex. 1002 ¶¶ 92–93).

On this preliminary record, the '951 patent specification supports Petitioner in several places by consistently tying data acceleration to stacking techniques that include contacts through the stacked dies. *See* Ex. 1001, 2:65–3:2 ("[T]he FPGA module may employ stacking techniques to combine it with a memory die for the purpose of accelerating external memory references as well as to expand its on chip block memory."), 2:28– 60 (describing wafer thinning so "metal contacts can traverse the thickness of the wafer" to create "a single very compact structure" and ultimately "accelerat[e] the sharing of data between the microprocessor and FPGA"), 2:63–65 ("Further disclosed herein is an FPGA module that uses stacking techniques to combine it with a memory die for the purpose of accelerating external FPGA reconfiguration"); *see* Pet. 30 (citing Ex. 1001, 2:65–3:2; Ex. 1007, 17, 19; Ex. 1002 ¶ 93).

Moreover, the '951 patent does not describe a wide configuration data part as part of a memory array. *See* Ex. 1001, Fig. 5 (showing box 82 as including a wide configuration data port for accessing logic cells in memory of an FGPA), 4:9–13 (describing Fig. 5 as a "functional block diagram" for a "reconfigurable processor module"); *cf.* Prelim. Resp. 17 (arguing "a memory array functional to accelerate external memory references" requires "a memory array—not a large number of contact points" to be functional to accelerate the memory references). On this preliminary record, as discussed further below, multiple contact points on or through the memory array die, connected to the memory array and processing element, render the "memory array

functional to accelerate external memory references to the processing element" as required by claim 1.

For purposes of institution, Petitioner shows that the advantages of die stacking using contacts extending through the dies were well-known, and include "high speed" and "parallel signal processing." *See* Pet. 4 (citing Ex. 1010, 1704; Ex. 1002 ¶ 39). This speed (or data acceleration) arises from shorter signal paths using the contacts extending through dies as opposed to longer contact runs at the periphery. *See* Pet. 15 (discussing Ex. 1009, 7:16– 34 (stacking with through-hole contacts minimizes latency and maximizes bandwidth)); Ex. 1006, 1 ("interconnect delay" occurs in prior art non- stacked FGPAs); Ex. 1010, 1704 ("High-speed performance is associated with shorter interconnection delay time and parallel processing. . . . High-speed performance is associated with shorter interconnection delay time and parallel processing.").

The abstract of the '951 patent also supports this interpretation. It specifically ties "stacking . . . die elements and "contacts that traverse the thickness of the die" to create a "processor module" with the claimed acceleration: "The processor module disclosed allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." Ex. 1001, code (57).

Figure 4 of the '951 patent, which follows, also supports this interpretation:

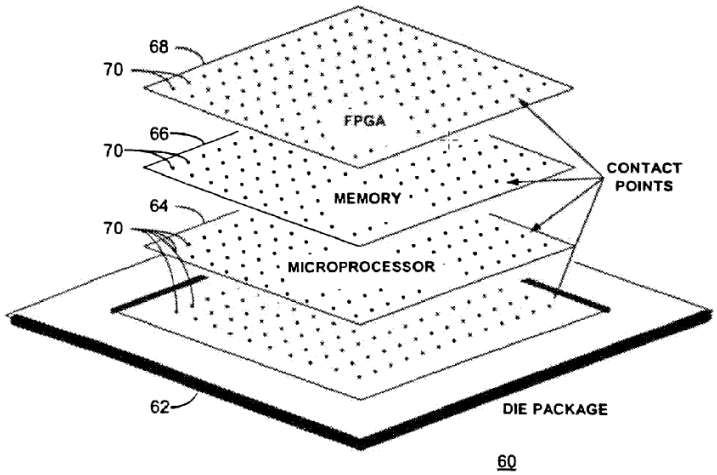


Fig. 4

As depicted above, Figure 4 shows a number of contact points within the periphery of each die (i.e., memory die, microprocessor die, and FPGA die). According to the abstract as quoted above, these "contacts . . . traverse the thickness of the die." Ex. 1001, code (57).

Accordingly, the claim construction of limitation [1.4] "a memory array functional to accelerate external memory references to the processing element," is "a number of vertical contacts that traverse the memory die in the internal periphery of the die and provide contacts on the surface of the memory die."

For purposes of institution, the claim construction of "said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array" as recited respectively in claims 5 and 10 is the same.

Finally, prosecution history plays an important role in understanding the claims and supports the preliminary claim construction. Under *Phillips*, "[l]ike the specification, *the prosecution history provides evidence of how the PTO and the inventor understood the patent*." *Phillips*, 415 F.3d at 1317 (emphases added). Here, the prosecution history provides some understanding of "wherein said memory array is functional to accelerate external memory references to said processing element." The Examiner indicated allowance of dependent claim 35 (if written in independent form) over Lin (U.S. Patent No. 6,451,626, finding Lin does not teach or suggest this "accelerate" limitation. *See* Ex. 1004, 68, 73–74; Pet. 8–9 (discussing prosecution history).

Addressing the prosecution history, Petitioner provides the following figures from Lin:

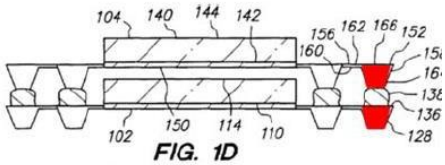


FIG. 1D

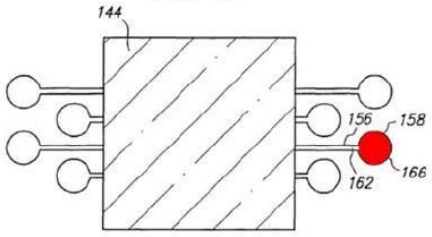


FIG. 2D

Petitioner's annotations of Lin's Figures 1D and 2D show that Lin discloses contacts on the sides of dies, instead of a number contact vias extending throughout the thickness of the dies. *See* Pet. 9 (citing Ex. 1019, Figs. 1D, 2D; Ex. 1004, 73).

Accordingly, in light of Lin's teachings and absent explicit explanation during prosecution by the Examiner, the rejection and reasons for allowance provide further support the understanding that the "functional to accelerate" limitations require a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and processor. *Compare*, Ex. 1001, Fig. 4 (showing numerous contact points), *with* Ex. 1019, Fig. 1D, 2D (showing peripheral contact points).

Based on the current record, no other terms require explicit construction. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'. . . ." (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness, Koyanagi and Alexander, Claims 1, 4, 5, 8, 10, 13–15*

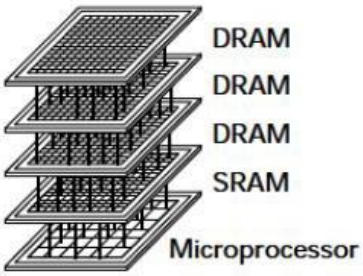
Petitioner *contends* the subject matter of claims 1, 4, 5, 8, 10, 13–15 would have been obvious over the combination of Koyanagi and Alexander. Pet. 17–46. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 16–20.

1. *Koyanagi*

Koyanagi describes a "three-dimensional integration technology" ("3D") that involves vertically stacking and interconnecting chips using "a high density of vertical interconnections" (Ex. 1007, 17) to "connect[] each layer (*id.* at 18).

Koyanagi explains that its 3D-integration technology "enables a huge number of metal microbumps to form on the top or bottom surfaces of the chips." *Id.* at 17–18 ("More than 10^5 interconnections per chip form in a vertical direction in these 3D . . . chips.") Koyanagi's system "dramatically increase[s] wiring connectivity while reducing the number of long interconnections." *Id.* at 17.

Koyanagi's Figure 1a follows:



(a)

Figure 1a illustrates a stack of chips including dynamic random access memory (DRAM) chips and a synchronous random access memory (SRAM) chip "stacked on a microprocessor" chip. *See* Ex. 1007, 17. Koyanagi describes "form[ing] as many vertical interconnections as possible" to "remove the generated heat" and form "electrical wirings." *Id.* According to one embodiment in Koyanagi, "2D image signals move simultaneously in a vertical direction and are processed in parallel." *Id.* at 18. Koyanagi also describes a variety of uses: "Typical examples of these new system LSIs include a merged logic memory (MLM) LSI chip as shown in Figure 1 . . . , and a 3D

shared memory for parallel processor systems." *Id.* at 17.

2. *Alexander*

Alexander describes "stacking together a number of 2D FPGA bare dies" to form a 3D FPGA. Ex. 1006, 1. Alexander explains that "each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die." *Id.*

Petitioner annotates Alexander's Figure 2 as follows:

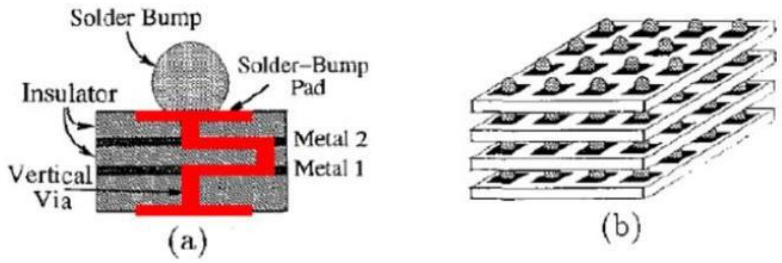


Figure 2(a) shows vertical metal connections (red) traversing a chip/die with a solder pad and bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1006, 1.

Alexander explains that stacking bare dies to form a 3D FPGA results in a chip with a "significantly smaller physical space," lower "power consumption," and greater "resource utilization" and "versatility" as compared to conventional layouts. Ex. 1006, 1.

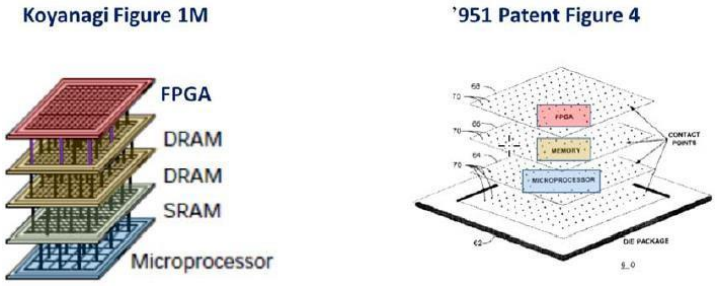
3. *Claims 1, 4, 5, 8, 10, 13, 14, and 15*

Claim 1's preamble recites "[a] processor module comprising." Petitioner relies on the combined teachings of Koyanagi and Alexander, providing

evidence that Koyanagi disclosing all elements of the claimed processor module, with the exception of a "programmable array." *See* Pet. 23–24.

Claim 1 also recites limitation [1.1], "at least a first integrated circuit functional element including a programmable array that is programmable as a processing element." *See* Pet. 24. Petitioner contends that Koyanagi and Alexander render the limitation obvious. *Id.* Petitioner relies on Alexander's FPGA, quoting Alexander as follows: "The FPGA can be visualized as programmable logic blocks embedded in programmable interconnect []. Unlike ASICs, the logic and interconnect resources are uncommitted, and can be configured to implement different logic functions and connectivity." Pet. 24 (quoting Ex. 1013, 6).

Petitioner provides the following modified version of Koyanagi's Figure 1 in a side-by-side comparison with the '951 patent's Figure 4:



Koyanagi's annotated Figure 1 (labeled 1M by Petitioner) shows a stack of dies with Alexander's FPGA die replacing one of Koyanagi's DRAMs, and the '951 patent's Figure 4 shows a structurally and functionally similar configuration. *See* Pet. 24.

Petitioner provides evidence that "FPGAs . . . can be flexibly configured and reconfigured to 'implement arbitrary logic' and thus 'provide designers with a faster and more economical design cycle.'" Pet. 18 (quoting Ex. 1006, 1; citing Ex. 1002 ¶ 76). Petitioner provides other reasons why a person of ordinary skill in the art ("POSITA") would have been motivated to employ Alexander's FPGA in a stack:

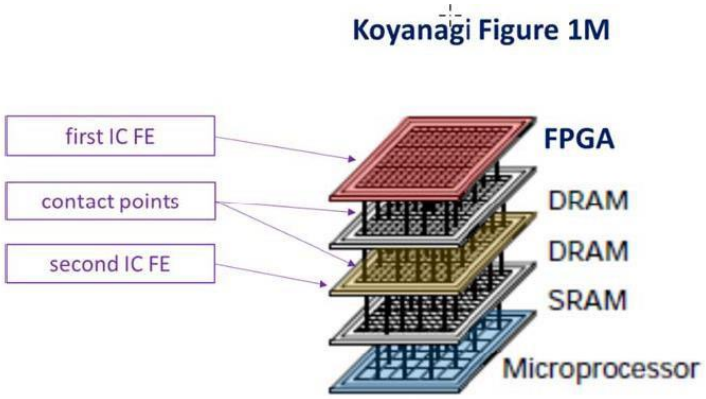
> A POSITA would have been motivated to apply Koyanagi's broadly applicable 3D integration scheme to stack Alexander's FPGA bare die over the memory and microprocessor die of Koyanagi Figure 1(a) to form a compact 3D reconfigurable module to save area, reduce power consumption, and improve performance. [Ex. 1002 ¶ 82]. A POSITA would have found it obvious to try such stacking and would have had a reasonable expectation of success doing so because both Alexander and Koyanagi teach the same 3D integration scheme whereby bare dies are stacked and interconnected using distributed through-silicon contacts, and because Koyanagi provides broadly applicable, detailed teachings with regard to stacking different types of dies. *Id.*; Ex. 1002 ¶ 82.

Pet. 22–23.

Petitioner also provides citations to Koyanagi and Alexander to support the showing that they include "common teachings" involving "the same 3D-integration scheme." *See* Pet. 17–23 (citing Ex. 1007, 17, 19, Figs. 1, 5; Ex. 1006, 1; Ex. 1002 ¶¶ 79–82; Ex. 1010, 1712–13 (citing advantages of a 3D stacking system including "minituarization, low power

consumption, and large-scale integration," and "speed and power dissipation").

Claim 1 also recites elements [1.2] "at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element" and [1.3]: "wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements." Petitioner's annotated version of Koyanagi Figure 1 depicts stacked functional elements and the coupled contact points relied upon by Petitioner:



Koyanagi's Fig. 1 above as annotated by Petitioner (as Fig. 1M) shows "the top FPGA die ('first IC FE') and the memory die ('second IC FE') . . . electrically coupled by a large number of contact points distributed throughout the surfaces of the functional elements." Pet. 26. To support this showing, Petitioner quotes Koyanagi: "More than 10^5 [100,000] interconnections per chip form in a vertical direction in these 3D LSI chips or 3D MCMs. Consequently, we can dramatically increase wiring connectivity while

reducing the number of long interconnections"). *Id.* at 26–27 (citing Ex. 1002 ¶ 87).

Petitioner relies on similar teaching in Alexander, including that Alexander "describe[s] 'a matrix of 100 x 100 = 10,000 solder bumps' formed over the surface of each die." Pet. 27 (quoting Ex. 1006, 1; citing Ex. 1002 ¶ 88; Ex. 1006, reproducing Ex. 1006, Figs. 2a, 2bs); *see supra* Section III.D.2 (Alexander's Figs. 2a, 2b showing vertical vias and solder bumps). Petitioner provides similar motivation to combine Alexander and Koyanagi as summarized above in connection with element [1.1]. *See* Pet. 17–23 (§ 7A.1: "**Reasons to Combine Koyanagi and Alexander**)."

Claim 1 also recites limitation [1.4]: "wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element." Petitioner relies on the combined teachings of Koyanagi and Alexander to address this claim limitation. According to Petitioner, the '951 patent "specification indicates that attributes the claimed acceleration to the stacking of an FPGA die and a memory die, whereby a wide configuration data port interconnects the stacked memory die and the FPGA using contact points distributed throughout the dies." Pet. 28 (quoting Ex. 1001, 2:65–3:2 ("[T]he FPGA module may employ stacking techniques to combine it with a memory die for the purpose of accelerating external memory references as well as to expand its on chip block memory"); citing Ex. 1001, 2:33–46). Petitioner contends that the combination of Koyanagi and Alexander "renders the claimed acceleration obvious because this prior art combination discloses the same

way to accelerate external memory references as is described in the '951 Patent specification." *Id.* (citing Ex. 1002 ¶ 90).

Petitioner also cites a number of known benefits that an increased number of vertical contacts provides, including "obtain[ing] more connections between the die" to mitigate bus bottlenecks common in conventional 2D layout, and to increase speed by providing more abundant and shorter circuit board wirings. *See* Pet. 30 (citing Ex. 1001, 2:65–3:2; Ex. 1007, 17, 19; Ex. 1002 ¶ 93). Petitioner provides other similar motivation to combine Alexander and Koyanagi as summarized above in connection with element [1.1]. *See* Pet. 17–23 (§ 7A.1: "**Reasons to Combine Koyanagi and Alexander**)."

First, regarding the "claimed programmable array," Patent Owner contends that "Petitioner fails to rely on a single teaching or citation from Alexander in support of their assertion that this claim element is met." Prelim. Resp. 17 (citing Pet. 28–30). This argument does not undermine Petitioner's showing. As summarized above, Petitioner relies on teachings in Alexander and cites to Alexander in addressing the "programmable memory array" as recited in limitation [1.1]. This teaching carries forward into the other limitations of claim 1.

Second, Patent Owner alleges that Petitioner fails to show that the DRAM memory of Koyanagi is "a memory array ***functional to accelerate external memory references to the processing element***." Prelim. Resp. 17. This argument also does not undermine Petitioner's showing. Patent Owner acknowledges that Petitioner "alleges that Koyanagi teaches a DRAM memory, and alleges that 'DRAM

includes a memory array' which they allege is well known in the art." Prelim. Resp. 17 (citing Pet. 28). Petitioner shows that it was well-known that DRAM memories include memory arrays. *See* Pet. 28 (citing Ex. 1002 ¶ 89; Ex. 1014, 151, Fig. 5.2); Ex. 1014, 149–52 (showing DRAMs and SRAMs as typical of one of "three major divisions of memories" such as RAMs, which consists of "bits arranged in an array"). Koyanagi's DRAMs, as depicted in Figure 1, appear as arrays (i.e., ordered rows and columns). *See* Ex. 1006, Fig. 1(a).

Third, Patent Owner alleges that Petitioner relies on a "require[d] . . . feature of a 'wide configuration data port' disclosed in the . . . '951 [p]atent [specification]." Prelim. Resp. 18 (citing Pet. 28). However, as discussed above, the claim construction does not require a wide configuration data port as a requirement of the claim. *See* Prelim. Resp. 18 ("To the extent that the Board agrees with Petitioner that this claim element requires a wide configuration data port, Koyanagi in view of Alexander does not teach a 'wide configuration data port,' let alone a wide configuration data port 'functional to accelerate external memory references to the processing element.'").

Patent Owner's claim construction argument does not undermine Petitioner's showing. The combined memory array of Koyanagi and Alexander as set forth by Petitioner includes a large number of contact points that perform the acceleration function. Pet. 28–29. As Petitioner argues, Petitioner's showing employs Koyanagi and Alexander in the same manner that the '951 patent employs stacked dies with a "large number of contact points distributed

throughout the surfaces of the dies." *Id.* at 29. Petitioner also cites to known advantages to stacking 3D chips with multiple vertical contacts including "high packing density," "high speed," "parallel signal processing," and "integration of many functions on a single chip." *See* Pet. 4 (citing Ex. 1010, 1704; Ex. 1002 ¶ 39). Koyanagi similarly discloses that multiple vertical contacts provides for parallel signal processing as indicated above. *See supra* Section III.D.1.

Finally, Patent Owner contends that Petitioner provides "general statements" and fails to show "any . . . motivation in the prior art . . . to arrive at the claim invention." Prelim. Resp. 21. According to Patent Owner, Petitioner's statement asserting "well-known benefits of miniaturization, lower power consumption, and large-scale integration, . . . is unrelated to how and why a POSITA would have modified *Alexander's* stacked FPGA to not only incorporate *Koyanagi's* DRAM memory and vertical interconnections but also to arrange those components such that they would be able to accelerate external memory references to an FGPA." *Id.* at 21–22 (quoting Pet. 21–22). Contrary to these arguments, Petitioner's statement and other above-discussed motivation statements relate to "how and why" an artisan of ordinary skill would have combined the stack die features of Koyanagi with the similar features of Alexander, to include the well-known FGPA, and it shows how the vertical interconnections employed in both references track the disclosed invention to obtain the claimed acceleration.

Based on the foregoing discussion, Petitioner sufficiently establishes for purposes of institution that

the combination of Koyanagi and Alexander renders claim 1 obvious. Relying partly on its showing with respect to claim 1, Petitioner provides a similar showing for independent claims 5 and 10, which largely track the limitations recited in claim 1. *See* Pet. 31–35, 37–44. Petitioner also presents a sufficient showing supported by the record with respect to dependent claims 4, 8, and 13–15. *See* Pet. 31, 36–37, 44–46. Patent Owner argues the claims together with claim 1 and does not separately address claims 4, 5, 8, 10, and 13–15. *See* Prelim. Resp. 16–23.

Accordingly, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to claims 1, 4, 5, 8, 10, and 13–15.

E. *Obviousness, Bertin and Cooke 1, 4, 5, 8, 10, and 13–15*

Petitioner contends claims 1, 4, 5, 8, 10, and 13–15 would have been obvious over the combination of Bertin and Cooke. *See* Pet. 46–61. Similar to Koyanagi, Bertin teaches stacking different types of chips, including logic chips, microprocessors, and controllers to minimize latency and maximize bandwidth and heat dissipation, using through-chip conductors. *See* Pet. 47 (citing Ex. 1009, 1:20–27, 6:49–51, 7:16–34; Ex. 1002 ¶¶ 118–120).

Bertin does not disclose an FPGA. Petitioner relies on Cooke to describe stacking chips, including FPGAs, microprocessors, and memory planes. *See* Pet. 48 (citing Ex. 1008, 2:3–11, 2:40–55, 3:13–18, Figs. 1, 2, 8A; Ex. 1002 ¶ 121). Petitioner contends it would have been obvious to use FPGAs in Bertin's 3D stacks to improve performance, area-efficiency, packing densities, and speed, and avoid interconnect delays.

See id. at 48– 49 (citing Ex. 1001, 1:36–2:9; Ex. 1006, 1; Ex. 1009, 2:61–65; Ex. 1002 ¶¶ 122–123). Petitioner also reads the claim limitations of the challenged claims on to the combined teachings of Bertin and Cooke, providing a detailed showing, supported by the references and expert testimony. *See id.* at 46–49.

Patent Owner presents similar arguments regarding Bertin and Cooke as it presented with respect to Koyanagi and Alexander. For example, Patent Owner contends that "a large number of contact points" as disclosed in the claimed combination is insufficient to teach a "memory array . . . functional to accelerate external memory references to the processing element." *See supra* Section III.D.C. For the reasons discussed above, this argument does not undermine Petitioner's showing.

Patent Owner also alleges that Bertin does not disclosure "a large number of contact points," and "[i]nstead, Bertin discloses that a few, limited, through chip conductors are necessary for its purposes." Prelim. Resp. 24 (quoting Ex. 1009, 7:22–34). Patent Owner's reliance on a single embodiment, which does not limit the number of contact points, does not undermine Petitioner's showing. Bertin generally discloses "through chip conductors" to connect to devices in chips without limitation. *See* Ex. 1001, 1:55. Bertin also teaches "the interconnections of the present invention provide high system packing densities and . . . provide low inductance, high performance inter-chip and intra-chip communication and heat dissipation." *Id.* at 2:61–65; Pet. 57–58 (citing Ex. 1009, 2:61–65).

As Petitioner argues, the '951 patent does not specify how many interconnections the claimed

"accelerate" functionality requires. *See* Pet. 56 (arguing that "neither the claim nor the specification describes a baseline from which to measure the claimed acceleration"). In any event, Petitioner provides sufficient reasons and shows the obviousness of using a large number of through-hole contacts. *See id.* at 56–58. For example, Petitioner relies partly on Bertin's teaching of using "any desired amount of through- chip conductors" in chips to "provide higher performance," including by connecting array drivers in one chip to array lines in a memory chip. *See* Pet. 57–58 (quoting Ex. 1009, 4:57–60, 6:38–48; citing Ex. 1009, 2:61–65; Ex. 1002 ¶ 136).

Patent Owner also contends that Petitioner does not "explain why a POSITA would be motivated to combine the Cooke's teaching of an FPGA stacked with memory planes into Bertin's teaching of through chip conductors" or "how such a combination would operate or that the modification would have been within the skill of a POSITA." Prelim. Resp. 26. These arguments do not undermine Petitioner's showing. Petitioner shows on this limited record that given the skill level involved here, an artisan of ordinary skill readily could have employed through-hole contacts to memory arrays using Bertin's and Cooke's stacked die techniques, where the advantages of FPGA's, stacked chips, and through-hole contacts were well-known. *See* Pet. 46–58; *supra* Section III.B (level of ordinary skill).

Based on the foregoing discussion and a review of the record, for purposes of institution, Petitioner sufficiently shows that the combination of Bertin and Cooke renders obvious the subject matter of claim 1. Petitioner also sufficiently shows that the

combination of Bertin and Cooke renders obvious the subject matter of claims 4, 5, 8, 10, and 13–15. *See* Pet. 46–61. Patent Owner argues the claims together with claim 1 and does not separately address claims 4, 5, 8, 10, and 13–15. *See* Prelim. Resp. 23–26.

Accordingly, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to claims 1, 4, 5, 8, 10, and 13–15.

III. CONCLUSION

After considering the evidence and arguments presented in the Petition and the Preliminary Response, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail with respect to its unpatentability challenges. Accordingly, we institute an *inter partes* review on all of the challenged claims and all of the grounds presented in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of these challenged claims.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, *inter partes* review is instituted as to the challenged claims of the '951 patent with respect to all grounds of unpatentability presented in the Petition; and

FURTHER ORDERED that *inter partes* review is commenced on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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APPENDIX C

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case IPR2020-01022
Patent 6,781,226 B2

SAMSUNG ELECTRONICS, CO., LTD., PETITIONER,

v.

ARBOR GLOBAL STRATEGIES, LLC, PATENT OWNER.

Entered: Dec. 2, 2020

DECISION

Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

FENICK, *Administrative Patent Judge*.

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 13, 14, 16–23, and 25–30 (the "challenged claims") of U.S. Patent No. 6,781,226 B2 (Ex. 1001, "the '226 patent"). Petitioner filed a Declaration of Dr. Stanley Shanfield (Ex. 1002) with its Petition. Arbor Global Strategies LLC ("Patent Owner"), filed a Preliminary Response (Paper 7, "Prelim. Resp."). Pursuant to the Board's Order

(Paper 8), the parties filed additional briefing to address the Board's discretionary authority to deny a petition based on a parallel district court proceeding under 35 U.S.C. § 314(b). Paper 9 ("Pet. Prelim. Reply"); Paper 10 ("PO Prelim. Sur-reply").

The Board has authority to determine whether to institute an *inter partes* review ("IPR"). *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), we may not authorize an *inter partes* review unless the information in the Petition and the Preliminary Response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we institute an *inter partes* review as to the challenged claims of the '226 patent on all grounds of unpatentability presented.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. Pet. 65. Patent Owner identifies Arbor Global Strategies LLC. Paper 5, 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC* v. *Samsung Electronics Co., Ltd. et al.,* 2:19-cv-00333-JRG-RSP (E.D.Tex.) (filed October 11, 2019) ("District Court" or "District Court Action") and *Arbor Global Strategies LLC v. Xilinx, Inc.*, 1:19-cv-1986 (D. Del.) as related proceedings. *See* Pet. 65–66; Paper 5, 1.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in two related

patents, respectively IPR2020-01020 challenging U.S. Patent No. RE42035 ((“the ’035 Patent”)) and IPR2020- 01021 (challenging U.S. Patent No. 7,282,951 (“the ’951 Patent”)).

C. *The ’226 patent*

The ’226 patent describes a stack of integrated circuit (“IC”) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the ’226 patent, this arrangement “allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” *Id.*

Figure 4 follows:

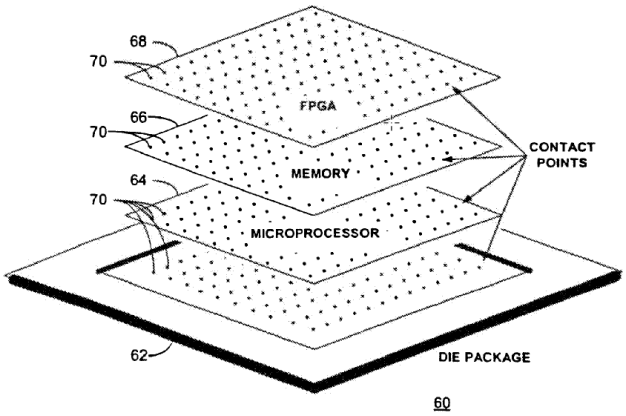

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64, interconnected using contact holes 70. Ex. 1001, 4:9–33.

The '226 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:19–35. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See id.* A "reconfigurable processor" provides a known benefit of flexibly providing the specific functional units needed for applications to be executed. *See id.*

D. *Illustrative Claims 13 and 22*

The Petition challenges independent claims 13 and 22, and claims 14, 16–21, 23, and 25–30, which depend from one of the challenged independent claims either directly or indirectly. Claims 13 and 22, reproduced below with bracketed numbering added for reference, illustrate the challenged claims at issue:

13. A processor module comprising:

[13.1] at least a first integrated circuit die element including a programmable array;

[13.2] at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

[13.3] at least a third integrated circuit die element including a memory stacked with

and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[13.4] means for reconfiguring the programmable array within one clock cycle.

Ex. 1001, 7:9–21.

22. A processor module comprising:

at least a first integrated circuit die element including a programmable array and a plurality of configuration logic cells;

at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and [22.4] means for updating the plurality of configuration logic cells within one clock cycle.

Ex. 1001, 8:4–17.

E. *The Asserted Grounds*

Petitioner challenges claims 13, 14, 16–23, and 25–30 of the '226 patent on the following grounds (Pet. 2):

Claims Challenged	35 U.S.C. §	References
13, 14, 16–23, and 25–30	103[1]	Koyanagi[2], Cooke[3]
13, 14, 16–23, and 25–30	103	Bertin[4], Cooke

II. DISCRETION TO DENY INSTITUTION UNDER § 314(a)

Patent Owner argues that "[t]he Board should deny the Petition because institution of this proceeding under § 314(a) because it would not be consistent with the objective of the AIA to 'provide an effective and efficient alternative to district court litigation.'" Prelim. Resp. 3 (quoting *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential) ("*NHK*").

In *NHK*, the Board declined to institute *inter partes* review, in part, because "under the facts and circumstances," a review "would be an inefficient use of Board resources," given the status of a parallel

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[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of institution, the '226 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

[2] M. Koyanagi et al., "Future System-on-Silicon LSI Chips," IEEE Micro, Vol. 18, Issue 4, July/August 1998. (Ex. 1007).

[3] Cooke, US 5,970,254, issued Oct. 19, 1999 (Ex. 1008).

[4] Bertin, US 6,222,276 B1, issued Apr. 24, 2001 (Ex. 1009).

district court proceeding between the same parties. *NHK*, Paper 8 at 20. The Board considered the following factors in *NHK*: (1) based on the district court's schedule, the district court's trial would conclude "before any trial on the [p]etition concludes"; and (2) the petitioner relied on the "same prior art and arguments" as its district court invalidity contentions, so the Board would "analyze the same issues" as the district court. *Id.* at 19–20.

As with other non-dispositive factors considered for institution under § 314(a), the Board weighs an early trial date as part of a "balanced assessment of all relevant circumstances in the case, including the merits." Patent Trial and Appeal Board Consolidated Trial Practice Guide 58 & n.2 (Nov. 2019), https://www.uspto.gov/TrialPracticeGuideConsolidated ("CTPG") (discussing follow-on petitions and parallel proceedings, citing *NHK* and *General Plastic Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017) (precedential)); *see Abbott Vascular, Inc. v. FlexStent, LLC*, IPR2019-00882, Paper 11 at 31 (PTAB Oct. 7, 2019) (declining to adopt a bright-line rule that an early trial date alone requires denial in every case).

Non-dispositive factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (order analyzing *NHK* issues) (precedential) ("*Fintiv*"). Overlap among these factors often exists and some facts may be relevant to more than one factor. *See id.* Therefore, in evaluating the factors, the Board holistically views whether denying

or instituting review best serves the efficiency and integrity of the system. *See* CTPG at 58 (quoting 35 U.S.C. § 316(b)); *Fintiv*, Paper 11 at 6.

The precedential *Fintiv* order lists the following factors for consideration "when the patent owner raises an argument for discretionary denial under *NHK* due to an earlier trial date": 1) whether a stay exists or is likely to be granted if a proceeding is instituted; 2) proximity of the court's trial date to the Board's projected statutory deadline; 3) investment in the parallel proceeding by the court and parties; 4) overlap between issues raised in the petition and in the parallel proceeding; 5) whether the petitioner and the defendant in the parallel proceeding are the same party; and 6) other circumstances that impact the Board's exercise of discretion, including the merits. *See Fintiv*, Paper 11 at 5–16.

1. *Factor 1–Likelihood of Stay*

Patent Owner notes that the District Court denied Petitioner's motion to stay the District Court Action. Prelim. Resp. 4 (citing Ex. 2001 (motion to stay); Ex. 2002 (denial)). Patent Owner contends that a stay "is highly unlikely" (*id.*) because the District Court informed that parties that Petitioner "may need to show that the Board is likely to invalidate every asserted claim—a showing that may require more than just pointing to a successful petition" (*id.* (quoting Ex. 2002, 6)). Patent Owner also argues that the District Court informed the parties that "Petitioner would only be permitted to refile the Motion 'if the Board institutes on all three Samsung petitions for *inter partes* review.'" *Id.* at 4 (quoting Ex. 2002, 5).

Analyzing the motion to stay, the District Court noted that the burden to show that a stay is appropriate had not been met "most importantly" because the Petitioner could not show that we had granted review on the Petitioner's three petitions for *inter partes* review. Ex. 2002, 3. The District Court noted that in *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018), the Supreme Court prohibited the Board's prior "partial institution" practice wherein "the Board would institute on a claim-by-claim basis, determining whether a particular claim had a reasonable likelihood of being invalidated." Ex. 2002, 5–6. The District Court then reasoned that "[s]ince the PTAB can no longer partially institute IPR proceedings, institution decisions may not be as useful as they were in the past for providing an indication of whether all [challenged] claims would be found unpatentable."

The Board herein determines that Petitioner has shown a reasonable likelihood of prevailing on all of the challenged claims. Certain dependent claims recite well-known circuitry or structure, including a microprocessor, a memory array, or a programmable memory array reconfigurable as a processing element, additional distributed contact points, or die elements thinned to a point at which contact points traverse the thickness of die elements. *See* claims 16–18, 25–27.

Because the Board institutes on all three petitions and Petitioner sets forth a strong showing of unpatentability on all of the challenged claims as discussed further below and in the two other concurrent decisions to institute (IPR2020–01020, Paper 11; IPR2020-1021, Paper 11), the record indicates that, although Petitioner's motion for a stay

was denied, the District Court is likely to allow Petitioner to refile a motion for a stay and may grant it under the circumstances presented here. *See* Ex. 2002, 5. Accordingly, *Fintiv* factor 1 weighs slightly in favor of not exercising our discretion to deny institution.

2. *Factor 2–Trial Date Versus FWD Due Date*

Patent Owner contends that "[t]his parallel proceeding has been pending for nearly a year. During that time, the court set a case schedule, and trial is set to begin April 5, 2021, ***eight months before*** a Final Written Decision would be expected to issue." Prelim. Resp. 5.

When a district court's trial date will occur before the projected statutory deadline, the Board generally weighs this factor in favor of exercising authority to deny institution under § 314(a). *Fintiv*, Paper 11 at 9.

The fact that the District Court is likely to allow Petitioner to refile a motion for stay and may grant a stay creates uncertainty as to whether the trial actually will start on the presently scheduled date, and diminishes the extent to which this factor weighs in favor of exercising discretion to deny institution. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 9–10 (June 16, 2020) (informative) ("[B]ecause of the number of times the parties have jointly moved for and the district court agreed to extend the scheduling order dates . . . and the uncertainty that continues to surround the scheduled trial date, we find that this factor weighs marginally in favor of not exercising discretion to deny institution under 35 U.S.C. § 314(a)").

Given that the District Court's currently scheduled trial date falls roughly eight months prior to the projected statutory deadline for a final written decision, but accounting for the uncertainty due to a possible stay as to whether the trial actually will start on the currently scheduled date, *Fintiv* factor 2 weighs moderately in favor of exercising our discretion to deny institution.

3. *Factor 3–Investment in Proceedings*

Patent Owner contends "by the time the Board is due to issue its institution decision in this case, claim construction and fact discovery will have been completed." Prelim. Resp. 6 (citing Ex. 2003, 3). According to Patent Owner,

> [t]he parties have also already filed their Joint Claim Construction and Prehearing Statement. Ex. 2005. Claim Construction briefing and the Markman Hearing will be completed by November 10, 2020. Ex. 2003. Fact discovery closes shortly thereafter—on November 16, 2020. *Id*. Expert discovery is expected to close on December 21, 2020, which is roughly two weeks after the Board is due to issue its institution decision in this case. *Id*. Accordingly, even if the Board finds that one or more of the grounds asserted in this Petition raises a reasonable likelihood that a claim is unpatentable, the parties will have already concluded expert discovery before a single post- institution brief is filed in this case.

Prelim. Resp. 7.

The District Court's original scheduling order generally supports Patent Owner's timeline. *See* Ex.

2003. After the parties completed the supplementary briefing, the District Court issued a first amended docket control order, which moves the close of fact discovery to December 7, 2020, and the close of expert discovery to January 5, 2021. *See* Ex. 3002, 2. According further to Patent Owner, "[p]ursuant to that [original] Order and the Court's Patent Rules, Patent Owner served its preliminary infringement contentions, Petitioner served its invalidity contentions, and Patent Owner served corrected infringement contentions." Prelim. Resp. 7 (citing Ex. 2003).

The Board considers the overlap of investment prior to the institution decision. The record shows that the parties and the District Court invested some resources in the parallel district court litigation albeit with respect to the three related patents noted (*supra* § I.B) with some portion of the work relevant to patent validity of the '226 patent. For example, Petitioner argues and the District Court docket control order indicates that Petitioner served its invalidity contentions on May 4, 2020, about two months after Patent Owner served its infringement contentions on March 9, 2020. Ex. 2003, 4; Pet. 65. The docket control order also lists August 25, 2020 and September 8, 2020 respectively as the dates for filing amended pleadings and a response to the amended pleadings. *See* Ex. 2003. The parties do not inform the Board if the amended pleadings listed on the District Court's order correspond to the date Patent Owner "served corrected infringement contentions." *See* Prelim. Resp. 7. In any event, Petitioner filed the instant Petition on May 29, 2020—about 3.5 weeks after it served its initial invalidity contentions on May 4,

2020, the due date ordered by the District Court. *See* Ex. 2003.

Also, according to Patent Owner, "Patent Owner filed its Complaint for infringement on October 22 [sic], 2019.[5] Ex. 2004. Then, on February 6, 2020, Petitioner filed a Motion to Dismiss, which the Court denied on April 20, 2020. *See* Ex. 2002. Following a hearing on March 23, 2020, the court entered a Docket Control Order. Ex. 2003." Prelim. Resp. 6. Therefore, assuming a service date of sometime between October 11–22, 2019 (*see supra* note 5), Petitioner filed the instant Petition on May 29, 2020—over 4 months prior to the statutory time bar date (one year after date of service) under § 315(b). Furthermore, according to Patent Owner's timeline, Petitioner filed the Petition a little over 5 weeks after the District Court ruled on Petitioner's motion to dismiss. *See* Prelim. Resp. 6.

Petitioner's timing as outlined above mitigates this *Fintiv* factor. If a petitioner, "faced with the prospect of a looming trial date, waits until the district court trial has progressed significantly before filing a petition," that decision "may impose unfair costs to a patent owner." *Fintiv*, Paper 11 at 11. On the other hand, "[i]f the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution." *Id.*

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[5] According to the District Court, Patent Owner filed the complaint on October 11, 2019. Ex. 2002, 1. The parties do not indicate the date of service of the complaint.

As discussed further in the next section, Petitioner's stipulation (Ex. 1025) minimizes the overlap or investment relative to the grounds in the IPR versus the invalidity challenges in the District Court Action. *See* Pet. Prelim. Reply 3.

("[B]ecause of Petitioner's stipulation, [the District Court] will not need to consider invalidity arguments based on the instituted grounds or grounds relying on the same primary reference as in the instituted grounds if the IPR is instituted."). Even though the Markman hearing already occurred (*see* Ex. 2003, Prelim. Resp. 7), the claim construction standard in the two proceedings is the same.

Considering the above-noted facts, including the time invested by the parties and court in the District Court Action, the extent to which the investment in the District Court Action relates to the issues of patent validity we would consider, and the timing of the filing of the Petition, this factor weighs slightly in favor of exercising our discretion to deny institution.

4. *Factor 4–Overlap of Issues*

This factor evaluates "concerns of inefficiency and the possibility of conflicting decisions" when substantially identical prior art is submitted in both the district court and the *inter partes* review proceedings. *Fintiv*, Paper 11 at 12.

Patent Owner argues that "the issues raised herein . . . overlap entirely with the art and issues raised the [D]istrict [C]ourt proceeding," so that "[t]his factor weighs very heavily in favor of discretionary denial." Prelim. Resp. 8 (citing Ex. 2006 (claim charts involving Koyanagi, Cooke and Bertin)). Petitioner responds it stipulated "that if the Board

institutes 'one or more of the IPR petitions on the grounds presented,' then Petitioner 'will not pursue those same instituted grounds or grounds based on the same primary reference' in the related district court litigation." Pet. Prelim. Reply 1 (quoting Ex. 1025 (stipulation)) (emphasis omitted).

Citing estoppel concerns under 35 U.S.C. § 315(e)(1), Patent Owner responds that "[a] meaningful stipulation in this case would have included not only the grounds and references actually raised in its Petition, but also all grounds that reasonably could have been raised." PO Prelim. Sur-reply 1 (citing *Sand Revolution*, Paper 24 at 12 n.5). Patent Owner adds that "[f]urthermore, Factor 4 concerns 'overlap between **issues raised** in the petition and in the parallel proceeding.'" *Id.* at 2 (quoting *Fintiv, Inc.*, Paper 11 at 6) (emphasis by Patent Owner).

Notwithstanding Patent Owner's arguments, Petitioner's stipulation here is broader than the stipulation in *Sand Revolution*, which states "if the IPR is instituted, Petitioner will not pursue the same grounds in the district court litigation." *Compare* Ex. 1025, 1–3, *with Sand Revolution*, Paper 24 at 11–12.[6] Like in *Sand Revolution*, Petitioner's stipulation here "mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as

[6] The stipulation here is broader than the stipulation in *Sand Revolution*, because although both stipulations preclude pursuing the "same grounds" in the *inter partes* reviews as the grounds employed in their respective district court trials, the stipulation here also precludes any "grounds based on the same primary reference" employed in the District Court.

well as concerns of potentially conflicting decisions." *Sand Revolution*, Paper 24 at 12.

In addition, the precedential *Fintiv* decision characterizes the precedential *NHK* decision as follows:

> In *NHK*, the patent owner argued the Board should deny institution under 35 U.S.C. § 314(a) because institution of a trial at the PTAB would be an inefficient use of Board resources in light of the "advanced state" of the parallel district court litigation *in which the petitioner had raised the same invalidity challenges*.

Fintiv, Paper 11 at 2 (quoting *NHK*, Paper 8 at 20) (emphasis added). And in *NHK*, in addition to relying on the advanced state of the district court trial to deny institution, the Board stated that in "[t]he district court proceeding, . . . Petitioner asserts *the same prior art and arguments*." *Id.* (emphasis added). The Board then reasoned "[i]nstitution of an inter partes review *under these circumstances* would not be consistent with 'an objective of the AIA . . . to provide an effective and efficient alternative to district court litigation.'" *Id.* (quoting *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, Case IPR2016-01357, Paper 19 at 16–17 (Sept. 6, 2017) (precedential as to § II.B.4.i) (emphasis added)).[7]

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[7] At least one Board member observed that *Fintiv* "says nothing about situations in which the petitioner is the same as, or is related to, the district court defendant." *Cisco Sys., Inc. v. Ramot at Tel Aviv Univ. Ltd.*, IPR2020- 00122, Paper 15 at 10 (PTAB May 15, 2020) (APJ Crumbley, dissenting). According to the dissent in *Cisco*, if "the factor weighs in favor of denial if the parties are the same," this could "tip the scales against a

Accordingly, *Fintiv* factor 4 weighs moderately in favor of not exercising our discretion to deny institution.

5. *Factor 5–Identity of Parties*

The District Court Action and the trial here involve the same parties. *See* Prelim. Resp. 8. "If a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact *against exercising discretion* to deny institution under *NHK*." *Fintiv*, Paper 11 at 13–14 (emphasis added).[7]

Accordingly, *Fintiv* factor 5 weighs slightly in favor of exercising our discretion to deny institution.

6. *Factor 6–Other Circumstances*

This final *Fintiv* factor represents a catch-all for any other relevant circumstances. Whether to exercise discretion to deny institution under § 314(a) involves "a balanced assessment of all relevant circumstances in the case, including the merits." CTPG 58.

Considering the parties' arguments in deciding the merits of the Petition and the Preliminary Response, Petitioner presents a strong showing on the merits here. In summary, on this preliminary record, Petitioner presents a strong showing stacking dies together with multiple contacts extending through the dies to connect circuits on the dies including processor, memory, FGPA circuits would have been obvious. *See infra* Section III.D–E; Pet. 17–63. In

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petitioner merely for being a defendant in the district court." *Id.* at 11. This "would seem to be contrary to the goal of providing district court litigants an alternative venue to resolve questions of patentability." *Id.*

other words, Petitioner shows that the challenged claims largely involve a "combination of familiar elements according to known methods . . . yield[ing] predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) ("The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results."). These predictable results include better performance in terms of speed, bandwidth, compactness, and power dissipation. *See infra* Section III.D–E; Pet. 17–63.

In addition, an IPR trial here avoids potentially complicated and overlapping jury issues of three related patents and allows the panel to focus on multiple issues in depth that involve not only the '226 patent, but also to consider related issues in the other two proceedings that may present a conflict with findings here. Therefore, this *inter partes* trial will provide the parties with an in-depth analysis of the '226 patent, providing a full record that will enhance the integrity of the patent system.

Accordingly, factor 6 weighs moderately in favor of not exercising our discretion to deny institution.

7. *Conclusion on § 314(a) Discretionary Denial*

Under *Fintiv*, the Board takes "a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Fintiv*, Paper 11 at 6. As discussed above, factor 2 weighs moderately and factors 3 and 5 weigh slightly in favor of exercising our discretion to deny institution. But factor 1 weighs slightly and factors 4 and 6 weigh moderately in favor of not exercising our discretion to deny institution.

Under a holistic analysis and under the particular circumstances of this case, the interests of efficiency and integrity of the patent system tilt toward not invoking our discretionary authority under § 314(a) to deny institution of the Petition.

III. ANALYSIS

Petitioner challenges claims 13, 14, 16–23, and 25–30 as obvious based on the grounds listed above. Patent Owner disagrees.

A. *Legal Standards*

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR*, 550 U.S. at 406. Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. *Level of Ordinary Skill in the Art*

Relying on the testimony of Dr. Shanfield, Petitioner contends that

> [a] person of ordinary skill in the art ("POSITA") at the time of the '226 Patent would have been a person having a Master's degree in Electrical Engineering, Computer Engineering, or Physics with three to five years of industry experience in integrated circuit design, layout, packaging or fabrication. Ex. 1002 ¶¶ 45–48. A greater level of experience in the relevant field may compensate for less education, and vice versa.

Pet. 7–8.

Patent Owner does not present a proposed level of ordinary skill or comment on Petitioner's proposal. For purposes of this Decision on Institution, we adopt Petitioner's proposed level of ordinary skill in the art, which comports with the teachings of the '226 patent and the asserted prior art.

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during

prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner and *Patent* Owner each agree that both "means for reconfiguring the programmable array within one clock cycle" (limitation 13.4 in claim 13) and "means for updating the plurality of configuration logic cells within one clock cycle" (limitation 22.4 in claim 22) are means- plus-function limitations and should be construed as per 35 U.S.C. § 112, ¶ 6. Pet. 9; Prelim. Resp. 11, 13.

Both of these limitations listed above recite "means" and further recite a function, thus creating a presumption that 35 U.S.C. § 112, ¶ 6 applies. *See* 35 U.S.C. § 112, ¶ 6 ("An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."); *see also Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (en banc in relevant part) (quoting *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 703 (Fed. Cir. 1998)) (holding that "use of the word 'means' creates a presumption that § 112, ¶ 6 applies"). We agree with the parties that these limitations are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6.

1. *Limitation 13.4 – "means for reconfiguring the programmable array within one clock cycle"*

The first step in construing a means-plus-function claim element is to identify the recited

function in the claim element. *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003)). The second step is to look to the specification and identify the corresponding structure for that recited function. *Id.*

Petitioner argues that the corresponding function for limitation [13.4] is "[r]econfiguring the programmable array within one clock cycle." Pet. 9–10. Patent Owner contends, however, that "within one clock cycle" is "a requirement of claim 1," but not part of the corresponding function for the means plus function claim limitation. Prelim. Resp. 11. Thus, Patent Owner contends that the corresponding function for the claim limitation is limited to "reconfiguring the programmable array." *Id.*

We note that, "[a] claim must be read in accordance with the precepts of English grammar." *In re Hyatt*, 708 F.2d 712, 714 (Fed. Cir. 1983). Additionally, "[35 U.S.C. § 112, ¶ 6] does not permit limitation of a means- plus-function claim by adopting a function different from that explicitly recited in the claim." *Micro Chem.*, 194 F.3d at 1258.

Patent Owner's argument that "within one clock cycle" is a requirement of the claim, without more explanation, does not describe how Patent Owner would interpret this requirement to be imposed. A construction where reconfiguration "within one clock cycle" describes how the "means for reconfiguring" of limitation 13.4 is used could raise the issue of claiming both a system and a method for using that system, and is therefore disfavored. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005) (a claim reciting both a system and the method for using that system does not apprise

a person of ordinary skill in the art of its scope); *Microprocessor Enhancement Corp. v. Tex. Instruments, Inc.*, 520 F.3d 1367, 1374–1375 (Fed. Cir. 2008) (holding a claim in means-plus-function format not indefinite as covering both an apparatus and method for use because, rather than describing of the use of the apparatus, the functional language related to "certain claimed features of the apparatus"); *Ruckus Wireless, Inc. v. Innovative Wireless Solutions, LLC*, 824 F.3d 999, 1004 ("If, after applying all other available tools of claim construction, a claim is ambiguous, it should be construed to preserve its validity.").

Reading the claim in accordance with the rules of grammar and as a claim covering an apparatus, we cannot discern how the phrase "within one clock cycle" would limit the claim, as Patent Owner argues, other than limiting the functioning of the claimed means. Therefore, on the present record and for the purposes of institution we conclude that "within one clock cycle" is properly part of the corresponding function for the means-plus- function limitation of claim 13.

We next review the '226 patent to determine what the structure is for the identified function. Petitioner proposes that the structure is "[a] wide configuration data port (82) interconnecting a stacked memory die (66) and FPGA die (68) using contact points (70) distributed throughout the die." Pet. 8 (citing Ex. 1001, 4:10–65, Figs. 4, 5). Patent Owner proposes that the corresponding structure is "a wide configuration data port." Prelim. Resp. 11–12 (quoting Ex. 1001, 4:45–59; citing *id* at 7:22–23 (claim 14)).

"While corresponding structure need not include all things necessary to enable the claimed invention to

work, it must include all structure that actually performs the recited function." *Default Proof Credit Card Sys. Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). Conversely, structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations. *Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc.*, 145 F.3d 1303, 1308–09, (Fed. Cir. 1998); *see B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997) ("[S]tructure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.").

In this case, Patent Owner's proposed corresponding structure leaves out certain structural features disclosed as performing the recited function. Patent Owner correctly characterizes the disclosure as contrasting Figure 3 with Figure 5, describing Figure 5 as showing how the FPGA "may be totally reconfigured in one clock cycle by updating all of the configuration cells 80 in parallel" and as showing that the operation of Figure 5 uses a wide configuration data port "[a]s opposed to the conventional implementation of FIG. 3" that includes "a relatively narrow, for example 8 bit[,] port." Ex. 1001, 4:45–54 (quoted at Prelim. Resp. 11–12), 4:7–9. But we look to the '226 patent and determine that there is more disclosure relating to what "actually performs the recited function." *Default Proof Credit Card*, 412 F.3d at 1298. The disclosure relating to Figure 5 continues beyond the portion cited by Patent Owner, describing that buffer cells in memory die 66 may be loaded while

the FPGA operates, and this loading "then enables the FPGA 68 to be totally *reconfigured in one clock cycle* with all of it[s] configuration logic cells 84 updated in parallel." Ex. 1001, 4:54– 59 (emphasis added). The functional connections allowing this "updat[ing] in parallel" from buffer cells to FPGA logic cells are shown in Figure 5, in which each buffer cell 88_n is connected to config memory cell 86_n and logic cell 84_n. *Id.* at Fig. 5. Logic cells 84 are comprised within FPGA 68 and buffer cells 88 preferably within a portion of memory die 66. *Id.* at 4:34–59. Further confirming that the connections between FPGA die 68 and memory die 66 are being referenced as part of the reconfiguration in one clock cycle, the disclosure continues directly from describing the updating in parallel to describe other uses "for taking advantage of the significantly increased number of connections to the cache memory die 66 [as shown in]FIG. 4[]," with respect to the FPGA die 68. *Id.* at 4:59–65. The implication is that the one clock cycle update of the FPGA, described immediately prior to this statement, also takes advantage of these connections. In light of this, we determine the structure should include, as Petitioner proposes, the interconnections between a programmable array die (the "first integrated circuit die element" of limitation 13.1) and a memory die (the "third integrated circuit die element" of limitation 13.3) as shown in Figures 4 and 5 and described in the associated disclosure (Ex. 1001, 4:10–5:4).

Patent Owner also argues that Petitioner's proposed structure "imports an FPGA into claim 13, which actually recites a 'programmable array.'" Prelim. Resp. 12; *see* Ex. 1001 7:9–21. On this point, we agree. While the '226 patent describes the

reconfiguration of a programmable array in one clock cycle in context of the reconfiguration of an FPGA, we seek to determine what structure from the written description is necessary to perform the claimed function. *Wenger Mfg., Inc. v. Coating Mach. Sys., Inc.*, 239 F.3d 1225, 1233 (Fed. Cir. 2001). In this case, the structure corresponding to the function is the wide configuration data port and interconnecting contact points between dies, not the particular type of programmable array on one of the dies.

Patent Owner argues that Petitioner's construction is incorrect because it is narrower than claim 14, or would render claim 14 obsolete if adopted. Prelim. Resp. 12. This argument is one of claim differentiation; "[u]nder the doctrine of claim differentiation, dependent claims are presumed to be of narrower scope than the independent claims from which they depend." *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1242 (Fed. Cir. 2003). However, our reviewing court has "long held" that a claim differentiation argument cannot be relied upon "to broaden a means-plus-function limitation beyond those structures specifically disclosed in the invention." *Safran v. Johnson & Johnson*, 712 F.3d 549, 563 (Fed. Cir. 2013).

For the reasons discussed above, on the present record and for the purposes of institution, we find that, for means-plus-function limitation 13.4 of claim 13, the function is "reconfiguring the programmable array within one clock cycle," and the corresponding structure is "a wide configuration data port interconnecting a memory and the programmable array using contact points distributed throughout the

first integrated circuit die element and the third integrated circuit die element."

2. *Limitation 22.4 – "means for updating the plurality of configuration logic cells within one clock cycle"*

Petitioner and Patent Owner refer back to or recapitulate their arguments with respect to limitation 13.4 in their arguments for the function and structure of means-plus-function claim limitation 22.4. Pet. 11–12; Prelim. Resp. 13–14. To support arguments regarding this claim term the parties cite no additional disclosure other than that previously discussed, and we agree that the previously discussed disclosure supports the construction of claim limitation 22.4. Claim 22 differs from claim 13 in several respects, including the inclusion of a plurality of configuration logic cells in the first integrated circuit die element. Limitation 22.4 differs from limitation 13.4 in its statement of function ("updating the plurality of configuration logic cells" rather than "reconfiguring the programmable array").

For the reasons presented above, on the present record and for the purposes of institution, we find that, for means-plus-function limitation 22.4 of claim 22, the function is "updating the plurality of configuration logic cells within one clock cycle," and the corresponding structure is "a wide configuration data port interconnecting a memory and the plurality of configuration logic cells using contact points distributed throughout the first integrated circuit die element and the third integrated circuit die element."

3. *No additional constructions*

Based on the current record, no other terms require explicit construction. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'. . . ." (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness, Koyanagi and Cooke, Claims 13, 14, 16–20, 22, 23, and 25–29*

Petitioner contends the subject matter of claims 13, 14, 16–20, 22, 23, and 25–29 would have been obvious over the combination of Koyanagi and Cooke. Pet. 17–40. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 17–26.

1. *Koyanagi*

Koyanagi describes a "three-dimensional integration technology" ("3D") that involves vertically stacking and interconnecting chips using "a high density of vertical interconnections" (Ex. 1007, 17) to "connect[] each layer (*id.* at 18).

Koyanagi explains that its 3D-integration technology "enables a huge number of metal microbumps to form on the top or bottom surfaces of the chips." *Id.* at 17–18 ("More than 10^5 interconnections per chip form in a vertical direction in these 3D . . . chips."). Koyanagi's system "dramatically increase[s] wiring connectivity while reducing the number of long interconnections." *Id.* at 18.

Koyanagi's Figure 1a follows:

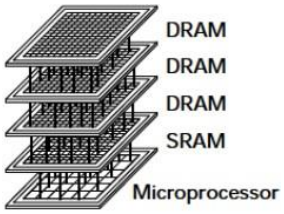


Figure 1a illustrates a stack of chips including dynamic random access memory (DRAM) chips and a synchronous random access memory (SRAM) chip "stacked on a microprocessor" chip. *See* Ex. 1007, 17. Koyanagi describes "form[ing] as many vertical interconnections as possible" to "remove the generated heat" and form "electrical wirings." *Id.* According to one embodiment in Koyanagi, "2D image signals move simultaneously in a vertical direction and are processed in parallel." *Id.* at 18. Koyanagi also describes a variety of uses: "Typical examples of these new system LSIs include a merged logic memory (MLM) LSI chip as shown in Figure 1 . . . , and a 3D shared memory for parallel processor systems." *Id.* at 17.

2. *Cooke*

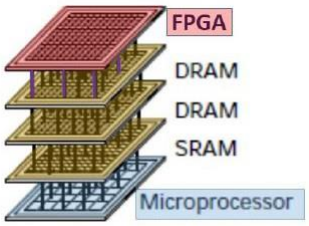
Cooke describes "[a] reconfigurable processor chip" with "a mixture of reconfigurable arithmetic cells and logic cells for higher effective utilization than a standard FPGA." Ex. 1008, code (57). "A configuration memory stack is provided, allowing for nearly instantaneous reconfiguration." *Id.* In Cooke, "[e]ach FPGA has two or more memory planes which can shift into the FPGA function in a single cycle." *Id.* at 2:45–49.

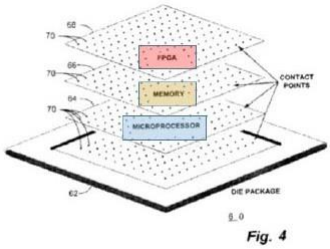
3. *Claims 13, 14, 16–20, 22, 23, and 25–29*

Claim 13's preamble recites "[a] processor module comprising." Petitioner relies on the combined teachings of Koyanagi and Cooke, providing evidence that Koyanagi discloses all elements of the claimed processor module, with the exception of the programmable array of limitation 13.1 and limitation 13.4's "means for reconfiguring the programmable array within one clock cycle." *See* Pet. 22–28. Petitioner provides reasons to combine Koyanagi and Cooke as discussed further below. *See id.* at 17–22.

Claim 13 also recites limitation 13.1, "at least a first integrated circuit die element including a programmable array," limitation 13.2, "at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element," and limitation 13.3, "at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively." Petitioner contends that the combination of Koyanagi and Cooke renders these limitations obvious. *Id.* at 23–25. Petitioner relies in part on Cooke's FPGA, citing Cooke's teaching of a standard processor and a reconfigurable FPGA on a single chip. *Id.* at 23 (quoting Ex. 1008, 2:1–2).

Petitioner provides the following modified version of Koyanagi's Figure 1(a) (on the left) in a side-by-side comparison with an annotated version of the '226 patent's Figure 4 (on the right):





Pet. 23. Petitioner's annotated version of Koyanagi's Figure 1 shows a stack of dies with Cooke's FPGA die replacing one of Koyanagi's DRAMs, and the '226 patent's Figure 4 shows a structurally and functionally similar configuration. *Id.* Petitioner contends that in the annotated version of Koyanagi's figure 1, the added FPGA from Cooke (in red) teaches the first integrated circuit die element of limitation 13.1, the microprocessor (in blue) teaches the claimed second integrated circuit die element of limitation 13.2, and the DRAM dies teach the claimed third integrated die element of limitation 13.3, with the electrical coupling of the layers (in limitations 13.2 and 13.3) indicated by the vertical lines between layers. *Id.* at 23–26 (citing Ex. 1008 2:1–7; Ex. 1007, 17; Ex. 1002 ¶¶ 74–77). To additionally support this showing, Petitioner quotes Koyanagi: "More than 10^5 [100,000] interconnections per chip form in a vertical direction in these 3D LSI chips or 3D MCMs. Consequently, we can dramatically increase wiring connectivity while reducing the number of long interconnections." *Id.* at 24 (citing Ex. 1002 ¶ 87).

Petitioner discusses how Cooke provides a tightly integrated FPGA with microprocessors and a "vertical stack" of memory planes. *Id.* at 18–19 (citing Ex. 1008, 20:40-55). Petitioner contends that Koyanagi's 3D integration scheme is "agnostic to the type and

functionality of the stacked dies." *Id.* at 18 (citing Ex. 1007, 17; Ex. 1002 ¶ 66). Petitioner provides reasons why a person of ordinary skill in the art ("POSITA") would have been motivated to employ Koyanagi's 3D integration teachings to achieve the benefits of vertically stacking the functional components of an FPGA- based reconfigurable computer system, such as the one described in Cooke:

> A POSITA would have been motivated to apply Koyanagi's broadly applicable 3D integration scheme to integrate the FPGA, memory and microprocessor components of Cooke's system into a compact single 3D chip because the stacked chip would save area, reduce power consumption, and improve performance. [Ex. 1002] ¶ 72. A POSITA would have found it obvious to try stacking the components of Cooke as taught by Koyanagi and would have had a reasonable expectation of success doing so because Cooke suggests a stacked system and Koyanagi provides broadly applicable, detailed teachings with regard to stacking different dies. *Id.*

Pet. 21–22.

Claim 13 recites element 13.4: "means for reconfiguring the programmable array within one clock cycle." Petitioner relies upon Cooke's disclosure of reconfiguring an FPGA in one clock cycle for the functional portion of limitation 13.4. Pet. 26 (citing Ex. 1002 ¶¶ 78–79; Ex. 1024, code (57); Ex. 1008, code (57), 2:47–48). For the corresponding structure, Petitioner relies on Koyanagi's vertical interconnections between stacked dies, and Cooke's disclosure that a large bandwidth allows configuration data from one memory plane to be

shifted into the FPGA in a single cycle. *Id.* at 27–28 (citing Ex. 1007, 17, Fig. 1(a); Ex. 1008, code (57), 2:47–48, 8:11–15; Ex. 1002 ¶ 79). Petitioner argues that Koyanagi as modified by Cooke "provides the same wide configuration data port" as described in the '226 patent, and that Cooke teaches how large data bandwidth allows the shift of configuration data in one clock cycle. *Id.* at 26–27 (citing Ex. 1002 ¶ 79).

Patent Owner presents several arguments relating to Petitioner's showing regarding limitation 13.4. First, Patent Owner argues that Koyanagi does not disclose a programmable array, "so it cannot disclose a wide configuration data port that reconfigures a programmable array on its own and Petitioner does not assert that *Cooke* cures this deficiency." Prelim. Resp. 18 (citing Pet. 18). This argument does not undermine Petitioner's showing. As summarized above, Petitioner relies on teachings in Cooke in combination with those in Koyanagi, and cites to Cooke in addressing the "programmable array" as recited in limitation [1.1]. This teaching carries forward into the other limitations of claim 1.

Second, Patent Owner alleges that Koyanagi does not teach a "wide configuration data port" but rather vertical interconnections used to transfer data between chips "without any details of how or why a POSITA would configure those interconnections into a wide configuration data port." Prelim. Resp. 18–19. However, Petitioner sufficiently describes the use of the vertical interconnections. Patent Owner presents no request for construction for the term "wide configuration data port," and the specification of the '226 patent indicates that a wide configuration data port allows the parallel updating of logic cells in the

FPGA through buffer cells in the memory die, which is consistent with Petitioner's arguments and evidence regarding vertical interconnections and Cooke's teachings for reconfiguring an FPGA in a single cycle. *See* Ex. 1001, 4:45–57; *see also* Ex. 1001, 4:59–65 (after describing the wide configuration data port, continuing with a description of "[o]ther methods for taking advantage of the significantly increased number of connections to the cache memory die"); Pet. 26–28. Patent Owner argues that "the type of vertical interconnections disclosed in Koyanagi are necessary but insufficient to teach a 'wide configuration data port' or its equivalent." Prelim. Resp. 19–20. Patent Owner further argues that the wide configuration data port "is facilitated by, but not coextensive with the existence of a large number of die area connections" but does not provide any further explanation of what more is required or cite support for this assertion. Prelim. Resp. 2. On the current record and for the purposes of institution, we determine that Petitioner's showing regarding the wide configuration data port is sufficient.

Finally, with respect to motivation to combine, Patent Owner contends that Petitioner provides only "general statements" and fails to show what would have led one of ordinary skill to modify the prior art references to arrive at the invention. Prelim. Resp. 22. Petitioner's statements, however, discussed above, are sufficiently specific. While Patent Owner faults Petitioner for not showing how one of ordinary skill "would have modified *Cooke's* shared memory stack to not only incorporate[] *Koyanagi's* vertical interconnections but also to arrange those interconnections into a wide configuration data port,"

Petitioner proposes not this modification, but rather the application of Koyanagi's 3D integration scheme to integrate the microprocessor components of Cooke's system. *Id.* at 22–23; *see, e.g.* Pet. 21–22.

According to Patent Owner, Petitioner's assertion that Koyanagi's 3D integration scheme for stacking dies is "agnostic to the type and functionality of the stacked dies" is incorrect and not stated or implied in the cited portions of Koyanagi. Prelim. Resp. 23–24 (citing Pet. 18). The Petition describes two different 3D stacked modules containing different types of dies used as examples in Koyanagi, and cites the testimony of its expert in support. Pet. 17–18 (citing Ex. 1007, 17–18, Figs. 1(a), 2; Ex. 1002 ¶¶ 65–66). Petitioner's showing regarding Koyanagi, including its expert's testimony, characterizing Koyanagi as "agnostic" with respect to the type of dies included in modules according to its 3D integration technology is, on the present record, sufficiently supported.

Based on the foregoing discussion, Petitioner sufficiently establishes for purposes of institution that the combination of Koyanagi and Cooke renders claim 13 obvious. Relying partly on its showing with respect to claim 13, Petitioner provides a similar showing for independent claim 22, which largely tracks the limitations recited in claim 1. *See* Pet. 36–38. Petitioner also presents a sufficient showing supported by the record with respect to dependent claims 14, 16–21, 23, and 25–30. *See* Pet. 28–35, 38–40. Patent Owner does not separately address claims 14, 16–21, 23, and 25–30. *See* Prelim. Resp. 17–26.

Accordingly, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to claims 13, 14, 16–23, and 25–30.

E. *Obviousness, Bertin and Cooke 13, 14, 16–23, and 25–30*

Petitioner contends claims 13, 14, 16–23, and 25–30 would have been obvious over the combination of Bertin and Cooke. *See* Pet. 40–62. Similar to Koyanagi, Bertin teaches stacking different types of chips, including logic chips, microprocessors, and controllers to minimize latency and maximize bandwidth and heat dissipation, using through-chip conductors. *See* Pet. 40– 41 (citing Ex. 1009, 1:20–57, 6:49–52, 7:17–34; Ex. 1002 ¶¶ 102–104).

Bertin does not disclose an FPGA. Petitioner relies on Cooke to describe stacking chips, including FPGAs, microprocessors, and memory planes. *See* Pet. 41–42 (citing Ex. 1008, 2:3–12, 2:40–55, 3:13–18, Figs. 1, 2, 8A; Ex. 1002 ¶¶ 105–106). Petitioner contends it would have been obvious to use FPGAs in Bertin's 3D stacks to improve performance, area- efficiency, packing densities, and speed, and avoid interconnect delays. *See* Pet. 42–43 (citing Ex. 1001, 1:36–2:9; Ex. 1006, 1; Ex. 1009, 2:61–65, 6:49–52; Ex. 1002 ¶¶ 106–107). Petitioner also reads the claim limitations of the challenged claims on to the combined teachings of Bertin and Cooke, providing a detailed showing, supported by the references and expert testimony. *See id.* at 43–62.

Patent Owner argues that Bertin only discloses stacking "similar chips," but that an FPGA, microprocessor, and memory are not similar chips. Prelim. Resp. 28 (quoting Ex. 1009, 7:16). Bertin describes the following:

> FIGS. 21 and 22 illustrate the ability to stack similar chips while providing high speed chip-to-

> chip connections through the silicon. As seen in FIG. 21, a stack of chips 142, 144, 146 and 148 is mounted directly on device 140, such as a logic chip, carry-card, microprocessor, controller, etc., to minimize latency between the device and chips and to maximize bandwidth.

Ex. 1009, 7:16–22. Patent Owner interprets this teaching as excluding "a stack including three different types of chips." Prelim. Resp. 28. Petitioner's interpretation of Bertin is that a variety of chips such as the recited logic chip or a microprocessor may be included in one stack of chips. *See* Pet. 16; Ex. 1002 ¶ 102. Bertin describes chips that differ, for example, in requiring different heights of chip-to-chip connectors, and it is not clear what similarity is required for the embodiment of Figures 21 and 22 in Bertin. *See* Ex. 1009, 6:49–7:15. While Patent Owner disagrees on the type or degree of similarity required for all chips in one stack in the Figures 21/22 embodiment of Bertin, we find Petitioner's explanation to be sufficiently supported, and find no indication that Bertin intended to require that the "similar" chips be of the same type.

Patent Owner also argues that Bertin does not disclose a large number of through chip conductors, but only that "a few, limited, through chip conductors are necessary for its purposes." Prelim. Resp. 28–29 (quoting Ex. 1009, 7:22–34). Patent Owner's reliance on a single embodiment, which does not limit the number of contact points, does not undermine Petitioner's showing. Bertin generally discloses "through chip conductors" to connect to devices in chips without limitation. *See* Ex. 1001, 1:55. Bertin also teaches "the interconnections of the present

invention provide high system packing densities and . . . provide low inductance, high performance inter-chip and intra-chip communication and heat dissipation." *Id.* at 2:61–65; Pet. 42–43 (citing Ex. 1009, 2:61–65).

Patent Owner presents similar arguments regarding Bertin and Cooke as it presented with respect to Koyanagi and Cooke. For example, Patent Owner contends that the means for reconfiguring the programmable array of limitation 13.4 is not taught because the combination of Bertin and Cooke does not disclose a "wide configuration data port." Prelim. Resp. 29–30. *See supra* Section III.D.3. For the reasons discussed above, this argument does not undermine Petitioner's showing.

Patent Owner also contends that Petitioner does not "explain why a POSITA would be motivated to combine [] Cooke's teaching of shifting memory into an FPGA function in a single cycle into Bertin's teaching of stacking similar chips and using through chip conductors" or "how such a *combination* would operate or that the modification would have been within the skill of a POSITA." Prelim. Resp. 31. These arguments do not undermine Petitioner's showing. Petitioner shows on this limited record that given the skill level involved here, an artisan of ordinary skill readily could have used Bertin's 3D integration teachings to provide improved performance and area-efficiency. *See* Pet. 40–43; *supra* Section III.B (level of ordinary skill).

Based on the foregoing discussion and a review of the record, for purposes of institution, Petitioner *sufficiently* shows that the combination of Bertin and Cooke renders obvious the subject matter of claim 13.

Petitioner also sufficiently shows that the combination of Bertin and Cooke renders obvious the subject matter of claims 14, 16–20, 22, 23, and 25–29. *See* Pet. 49–62. Patent Owner argues the claims together with claim 13 and does not separately address claims 13, 14, 16–20, 22, 23, and 25–29. *See* Prelim. Resp. 26–31.

Accordingly, we determine that Petitioner *establishes* a reasonable likelihood of prevailing with respect to claims 13, 14, 16–20, 22, 23, and

25–29.

III. CONCLUSION

After considering the evidence and arguments presented in the Petition and the Preliminary Response, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail with respect to its unpatentability challenges. Accordingly, we institute an *inter partes* review on all of the challenged claims and all of the grounds presented in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of these challenged claims.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, *inter partes* review is instituted as to the challenged claims of the '226 patent with respect to all grounds of unpatentability presented in the Petition; and

FURTHER ORDERED that *inter partes* review is commenced on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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APPENDIX D

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case IPR2020-01567[1]
Patent 7,126,214 B2

XILINX, INC., PETITIONER,

v.

ARBOR GLOBAL STRATEGIES, LLC, PATENT OWNER

Entered: Mar. 2, 2022

FINAL WRITTEN DECISION

35 U.S.C. § 318(a)

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

BENOIT, Administrative Patent Judge.

Xilinx, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–6 and 26–31 (the "challenged claims") of U.S. Patent No. 7,126,214 B2 (Ex. 1001, "the '214 patent"). Pet. 1. Petitioner filed a Declaration of Paul Franzon, Ph.D. (Ex. 1002) with its Petition. Arbor Global Strategies

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[1] Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00735 and has been joined as a party to IPR2020-01567.

LLC ("Patent Owner") filed a Preliminary Response (Paper 9, "Prelim. Resp."). We determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims, and on March 5, 2021, we instituted this proceeding as to all challenged claims and all grounds of unpatentability. Paper 13 ("Institution Decision" or "Inst. Dec.").

After institution, Taiwan Semiconductor Manufacturing Co. Ltd. ("TSM") filed a Petition seeking *inter partes* review of the claims challenged in this proceeding and a Motion for Joinder. IPR2021-00735, Papers 1, 3, 5.[2] We instituted an *inter partes* review in IPR2021-00735 and joined TSM as a party to this proceeding. Paper 20.

Subsequently, Patent Owner filed a Patent Owner Response (Paper 19, "PO Resp.") and a declaration of Shukri Souri, Ph.D. in support thereof (Ex. 2011); Petitioner filed a Reply (Paper 23, "Pet. Reply") and a supplemental declaration of Dr. Franzon in support thereof (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 27, "PO Sur-reply"). Thereafter, the parties presented oral arguments, and the Board entered a transcript into the record. Paper 33 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(b)(4). For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine

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[2] The petition in IPR2021-00735 (Paper 1) filed on April 5, 2021 was replaced by a corrected petition (Paper 5), which was accepted by the Board (Paper 7).

that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies itself (Pet. 48) and TSM identifies itself and TSMC North America (IPR2021-00735, Paper 5, 48). Patent Owner identifies Arbor Global Strategies LLC. Papers 4, 1; 6, 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies* LLC v. *Xilinx, Inc.,* 1:19- cv-1986-MN (D. Del.) (filed October 18, 2019) as a related proceeding. *See* Pet. 48; Papers 4, 1; 6, 1.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in three related patents, respectively IPR2020-01568 challenging U.S. Patent No. 7,282,951 ("the '951 patent"), IPR2020-01570 challenging U.S. Patent No. RE42035, and IPR2020-01571 challenging U.S. the 6,781,226 patent. *See, e.g.*, Pet. 48. These three patents also have been challenged by a different petitioner in IPR2020-01020, IPR2020-01021 ("IPR-1021"), and IPR2020-01022. The joined party here (TSM) also was joined as a party to each of those proceedings.

C. *The '214 patent*

The '214 patent describes a stack of integrated circuit ("IC") die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate

array, memory, and microprocessor. Ex. 1001, code (57), Fig. 4. According to the '214 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." Ex. 1001, code (57), Fig. 4.

Figure 4 follows:

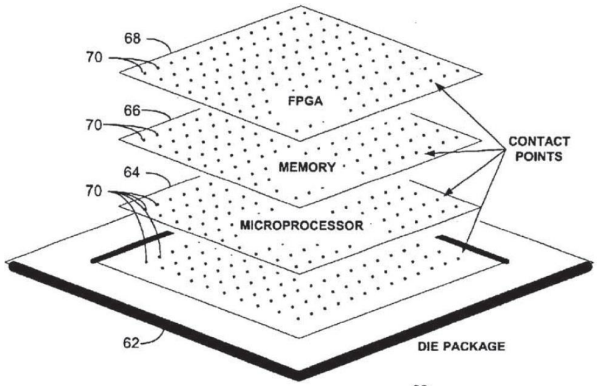

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 68, memory die 66, and microprocessor die 64, interconnected using contact holes 70. Ex. 1001, 4:59–5:2.

The '214 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:23–39. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See* Ex. 1001, 1:23–39. A "reconfigurable processor" provides a

known benefit of flexibly providing the specific functional units needed for applications to be executed. *See* Ex. 1001, 1:23– 39.

D. *Illustrative Claim*

The Petition challenges claims 1–6 and 26–31, of which claims 1, 2, 26, and 27 are independent claims. Each of the challenged claims are directed toward a programmable array module. *See, e.g.,* Ex. 1001, 7:56 (independent claim 1), 8:2 (independent claim 2), 9:41 (independent claim 26), 9:52. Claim 1, reproduced below with bracketed numbering added for reference, illustrates the challenged claims at issue:

1. A programmable array module comprising:

[1.1] at least a first integrated circuit functional element including a field programmable gate array; and

[1.2] at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element

[1.3] wherein said field programmable gate array is programmable as a processing element, and

[1.4] wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.

Ex. 1001, 7:56–67.

Among the differences recited by the independent claims, independent claims 2 and 27 recite "said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements." Ex. 1001, 8:1–15, 9:58–61. Independent claims 26 and 27 recite "wherein said memory array is functional to accelerate external memory references to said processing element." Ex. 1001, 9:49–51, 10:2–4.

E. *The Asserted Grounds*

Petitioner challenges claims 1–6 and 26–31 of the '214 patent on the following grounds (Pet. 1):

Claims Challenged	35 U.S.C. §	References
1, 2, 4, 6, 26, 27, 29, 31	103[3]	Zavracky[4], Chiricescu[5], Akasaka[6]
3, 28	103	Zavracky, Chiricescu, Akasaka, Satoh[7]

Claims Challenged	35 U.S.C. §	References
5, 30	103	Zavracky, Chiricescu, Akasaka, Alexander[8]

[3] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of institution, the '214 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

[4] Zavracky, US 5,656,548, issued Aug. 12, 1997 (Ex. 1003).

[5] Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98 (Ex. 1004).

[6] Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Issue 12, pp. 1703–14, Dec. 1986, ISSN 0018-9219 (Ex. 1005).

[7] Satoh, PCT App. Pub. No. WO00/62339, published Oct. 19, 2000. (Ex. 1008 (English translation)).

[8] Michael J. Alexander et al., *Three-Dimensional Field-Programmable Gate Arrays*, Proceedings of Eighth International Application Specific Integrated Circuits Conference, Sept. 1995 (Ex. 1009).

Petitioner contends that each of the asserted references is prior art to each of the challenged claims. Pet. 1–3.

II. ANALYSIS

Petitioner challenges claims 1–6 and 26–31 as obvious based on the grounds listed above. Patent Owner disagrees.

A. *Legal Standards*

To prevail in challenging Patent Owner's claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e) (2012); 37 C.F.R. § 42.1(d) (2017). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for inter partes review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied on).

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.[9] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

To demonstrate obviousness, "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418. More specifically, Petitioner must demonstrate by a preponderance of evidence that "a skilled artisan would have had reason to combine the teaching of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success from doing so." *PAR Pharm., Inc. v. TWI Pharm., Inc.*, 773 F.3d 1186, 1193 (Fed. Cir. 2014).

B. *Level of Ordinary Skill in the Art*

The parties dispute the level of ordinary skill in the art. The level of ordinary skill in the art is "a prism or lens through which . . . the Board views the prior art and claimed invention" to prevent hindsight bias. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). In determining the level of ordinary skill, various factors may be considered, including the

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[9] No argument or evidence regarding secondary considerations has been presented in this proceeding.

"types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovation are made; the sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.,* 57 F.3d 1573, 1579 (Fed. Cir. 1995) (internal quotation and citation omitted). Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm't, Inc*., 637 F.3d 1314, 1323 (Fed. Cir. 2011) ("A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.").

Relying on the declaration testimony of Dr. Franzon, Petitioner contends that

> [a] person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '214 patent would have been a person with a Bachelor's Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication. Ex. 1002 ¶¶ 58–60.

Pet. 7 (citing Ex. 1002 ¶¶ 58–60).

Patent Owner asserts that

> [a] person of ordinary skill in the art ("POSITA") around December 5, 2001 (the earliest effective filing date of the '214 Patent) would have had a Bachelor's degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field. Souri Decl., ¶ 25.

PO Resp. 8–9 (citing Ex. 2011 ¶ 25).

We adopt Petitioner's proposed level of ordinary skill in the art as we did in the Institution Decision, which comports with the teachings of the '214 patent and the asserted prior art. *See* Inst. Dec. 7. Patent Owner's proposed level largely overlaps with Petitioner's proposed level while lacking some specificity found in Petitioner's proposed level. Even if we adopted Patent Owner's proposed level, the outcome would remain the same. *See* Pet. Reply 1 (indicating Dr. Franzon confirmed his opinions under Patent Owner's proposed level of ordinary skill).

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under this standard, which is the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

In its Petition, Petitioner did not provide an express construction for any claim term. Pet. 13. Nor did Patent Owner in either its Preliminary Response or its Response to the Petition. Prelim. Resp. 5; PO

Resp. 9 (quoting 37 C.F.R. § 42.100(b)). In our Institution Decision, we agreed that no terms require explicit construction. Inst. Dec. 11–12 (citing Pet. 13; Prelim. Resp. 4, 5).

In that decision, we also noted and addressed the claim construction issue raised by Patent Owner in its Preliminary Response based on similar terms we construed in instituting trial in IPR-1021. Inst. Dec. 8–11. Specifically, Patent Owner argued the proper scope of the claim terms "said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element" recited in independent claims 1 and 2 and "said memory array is functional to accelerate external memory references to said processing element" recited in independent claims 26 and 27 (collectively, "the functional to accelerate" limitations). Inst. Dec. 8–11. We did not agree with Patent Owner's arguments and noted that the instituted trial would afford both parties an opportunity for further briefing the issue. Inst. Dec. 10–11.

During trial, the parties have disputed the scope of the "the functional to accelerate" limitations in the context of the purported teachings of the prior art and in their respective Reply and Sur-reply. *See, e.g.,* PO Resp. 19, Pet. Reply 2–3; PO Sur-reply 1–2. Patent Owner contends that the plain language of the challenged claims requires "that a memory array is responsible for the claimed acceleration of data references." PO Sur-reply 1. Each of the challenged independent claims recites "said memory array is functional to accelerate" either "reconfiguration of said field programmable gate array as a processing element" (claims 1 and 2) or "external memory

references to said processing element" (claims 26 and 27). Ex. 1001, 7:56–67 (claim 1), 8:1–15 (claim 2), 9:41–51 (claim 26), 10:2–4 (claim 27).

Patent Owner further contends that the structure within the memory array responsible for accelerating is the wide configuration data port disclosed in the '214 patent. PO Resp. 19 ("Rather, as the claims themselves require, it is a structure provided ***within the memory array*** (i.e. the wide configuration data port disclosed in the '214 Patent) that is responsible for accelerating the programmable array's accelerated memory references." (citing Ex. 2011 ¶ 53)); PO Sur-reply 2 (repeats statement that the wide configuration data port is the structure provided *within the memory array* that is responsible for the claimed acceleration (quoting PO Resp. 18–19)). Thus, Patent Owner equates (by using "i.e.") the requisite structure within the memory array to be the wide configuration data port disclosed in the '214 patent.

The challenged claims recite a function of the memory array and that that the memory array structurally is "stacked with and electrically coupled to" the FPGA. Ex. 1001, 7:59–60 (claim 1); *see also* Ex. 1001, 7:56–8:30 (claims 1, 2), 9:41–10:21 (claims 26, 27). None of the claims recite a wide configuration data port or any structure *within* the memory array.

For support, Patent Owner relies on Dr. Souri's declaration testimony. PO Resp. 19 (citing Ex. 2011 ¶ 53 (concluding that "it is the structure provided ***within the memory array*** (i.e. the wide configuration data port disclosed in the '214 Patent) that is responsible for accelerating the programmable array's accelerated external memory references")).

Prior to this conclusion, at the cited paragraph, Dr. Souri quotes a passage from the '214 patent specification, but that passage describes nothing about a memory array, and Dr. Souri provides no explanation for how he reaches this conclusory position. *See* Ex. 2011 ¶ 53 (quoting Ex. 1001, 5:16–26).

When explaining that position "[i]n more detail," Dr. Souri describes a wide configuration data port as interconnecting the two elements of a memory die and a programmable array die. Ex. 2011 ¶ 54 (describing the inventors as solving the problem of "unacceptably long reconfiguration times" "*by stacking a memory die with a programmable array die" and "by interconnecting those two elements with a 'wide configuration data port'* that employs through-silicon contacts, with the potential for even further acceleration where the memory die is 'tri-ported.'" (citing Ex. 1001, 5:16–26) (emphasis added here)). As such, Dr. Souri describes the wide configuration data port as *interconnecting a memory die and a programmable array die.* Although Dr. Souri describes the wide configuration data port as interconnecting two dies, Dr. Souri does not describe the wide configuration data port as being *within the memory array*. Because Dr. Souri does not adequately explain how a wide configuration data port *interconnecting a memory die* with another element shows a wide configuration data port *within a memory array*, we give little weight to Dr. Souri's testimony that the claims require a wide configuration data port *within* the memory array.

The weight we accord Dr. Souri's testimony in this regard is further supported by Patent Owner's

expert *Krishnendu* Chakrabarty, Ph.D. who indicates the very wide configuration data port shown in Figure 5 of the '214 patent connects the memory die and FPGA die.[10] Ex. 1075, 157:23–158:7; Ex. 1075, 156:7–10[11]; *see* Ex. 1075, 163:8–21 (describing a data port as "just an interface to send data from one place to another" and a configuration data port as "just a data port used for configuration")*; see also* Pet. Reply 9 (quoting 1075, 157:23–158:3, 163:8–163:21). Patent Owner argues its own prior expert's testimony contradicts the '214 patent description of "the wide configuration data port *with buffer cells*." PO Sur-reply 8 (citing Pet. Reply 9; Ex. 1001, 5:27–36) (emphasis added). For the reasons explained below, we do not agree that the '214 patent requires a wide configuration data port *to include buffer cells* and so do not agree with Patent Owner that Dr. Chakrabarty's description of a wide configuration data port contradicts the '214 patent.

Furthermore, the disclosure of a wide configuration data port in Figure 5 of the '214 patent does not support Patent Owner's position that the claims require such a structure *within* the memory array. The '214 patent depicts a "VERY WIDE CONFIGURATION DATA PORT 82" as a "black box"

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[10] Dr. Chakrabarty is Patent Owner's expert in the IPR2020-01020, IPR2020-01021, and IPR2020-01022 that challenge other patents of Patent Owner that have a substantially similar written description with regard to the cited portions of the '214 patent. *See* IPR2020-01020, Ex. 1001, Figs. 4–5; IPR2020-01021, Ex. 1001, Figs. 4–5; IPR2020-01022, Ex. 1001, Figs. 4–5.

[11] "Q: So in this system [referencing Fig. 4], the configuration data port has wires that connect the memory die to the FPGA die. Right? A: Yes."

in Figure 5 and is not clear on its face how the wide configuration data port 82 in Figure 5 relates structurally to a memory die or memory array. Ex. 1001, 5:27–37, Fig. 5. Additionally, Figure 5 of the '214 patent includes structures (specifically, buffer cells) described as preferably being within the memory die and structures (specifically logic cells) as being part of the FPGA. Thus, Figure 5 of the '214 patent does not depict the wide configuration data port 82 as being *within* a memory array.

Specifically, Figure 5 follows:

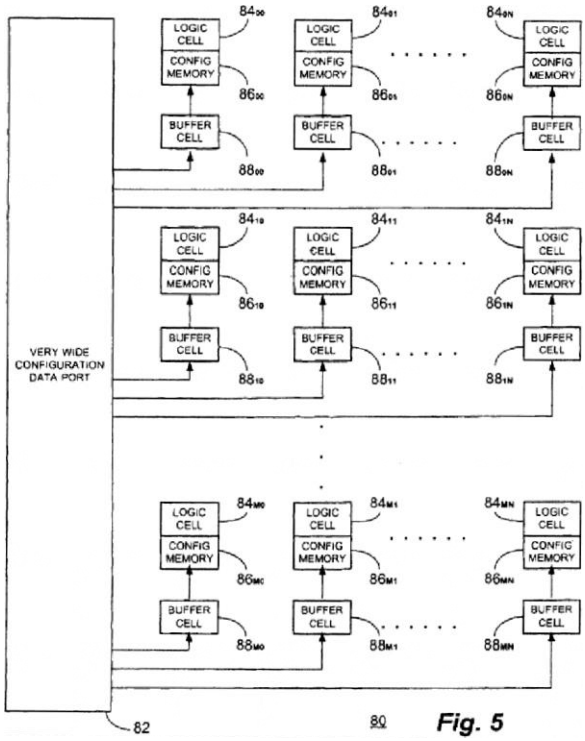

Fig. 5

Figure 5 shows a very wide configuration data port 82 on the left side of the figure that is connected to each buffer cell depicted to the right of very wide

configuration data port 82. *See* Ex. 1001, Fig. 5, 5:33–37. In turn, each buffer cell is connected to an associated configuration memory cell 86, which is adjacent to a logic cell 84. *See* Ex. 1001, Fig. 5, 5:33–37. The '214 patent indicates that "[t]he buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4)" but is silent as to the wide configuration data port's structural relationship to the memory die. Figure 5, however, depicts very wide configuration data port 82 as being separate from the buffer cells. Moreover, the '214 patent indicates that "the FPGA 68 compris[es] the logic cells 84," which are depicted in Figure 5 as being separate from the very wide configuration data port 82. Ex. 1001, 5:38.

Therefore, the '214 patent in Figure 5 and its corresponding description do not describe the wide configuration data port as being within the memory array. Ex. 1001, Fig. 5, 5:27–47. To the extent the claims implicate any portion of a wide configuration data port, it is the numerous via connections associated with that port connected to a memory die that supports a "memory array [] functional to accelerate" data references. This is consistent with the testimony of Patent Owner's experts Dr. Souri and Dr. Chakrabarty as outlined above.

Moreover, the '214 patent further indicates that Figure 5 is a "functional block diagram of the configuration cells" through which the FPGA 70 shown in Figure 4 is updated "in one clock cycle by updating all of the configuration cells in parallel."[12]

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[12] The '214 patent specification also states that "[f]urther disclosed herein is an FPGA module that uses stacking techniques to combine it with a memory die for the purpose of accelerating FPGA reconfiguration." Ex. 1001, 2:61–63. This, and

Ex. 1001, 5:27–33. Notably, the reconfigurable processor module 60 depicted in Figure 4 comprises "a die package 62 to which is coupled a microprocessor die 64, memory die 66 and FPGA die 68, all of which have a number of corresponding contact points, or holes 70 formed throughout the area of the package 62 and the various die 64, 66, and 68." Ex. 1001, 4:64–5:2. Thus, even in the embodiment describing the wide configuration data port 82 as part of Figure 4's reconfigurable processor module 60 that includes elements outside of memory die 66, the '214 patent does not indicate the wide configuration data port 82 is within a memory array. A wide configuration data port is not otherwise described in the '214 patent.

For these reasons, we find Figure 5's depiction of the wide configuration data port 82 does not support Patent Owner's position that a structure *within* the memory array is responsible for the recited acceleration.

In its Sur-reply, Patent Owner contends that the '214 patent "describes that the memory array is functional to accelerate when it describes a wide configuration data port and 'buffer cells 88 . . . a portion of memory die 66' (a necessary part of the wide configuration data port) that is responsible for the

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other disclosures, indicate that reconfiguration may occur by using the significant number of vias of the stacking technique (i.e., without necessarily requiring any other structure of Figure 5's wide configuration data port (whatever it is)). *See id.* at 5:41–47 ("Other methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory ("RAM" than can be offered within the FPGA die 68 itself.")).

acceleration of reconfiguration data to the field programmable gate array ('FPGA')[sic]." PO Surreply 1–2 (citing Ex. 1001, 5:32–41 (discussing Fig. 5)). The Patent Owner appears to be contending that the buffer cells 88 depicted in Figure 5 both (i) are a portion of memory die 66 and (ii) are a necessary part of the wide configuration data port. *See also* PO Resp. 21 (indicating the '214 patent "discloses utilizing a portion of the memory array as a wide configuration data port including buffer cells" (citing Ex. 1001, 5:33–38)); Tr. 53:18–19 (Patent Owner confirming its position that "buffer cells are part of the wide configuration data port.").

For the reasons discussed above, we do not agree that Figure 5 depicts the buffer cells as part of the wide configuration data port. The '214 patent expressly describes the central purpose of the buffer cells: "*they can be loaded while the FPGA 68 comprising the logic cells are in operation*," which "then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it[s] configuration cells 84 updated in parallel." Ex. 1001, 5:39–43 (emphasis added). None of the challenged claims, however, recite buffer cells or require that the recited FPGA be reconfigured while in operation.

Additionally, Patent Owner's edited quotation omits the qualification that "[t]he buffer cells are *preferably* a portion of the memory die 66" shown in Figure 4, which further undermines Patent Owner's position. Ex. 1001, 5:36–37. Additionally, the buffer cells are only "preferably a portion of the memory die 66" that enables loading the buffer cells while the logic cells are in operation. Ex. 1001, 5:36–39 ("The buffer cells 88 are preferably a portion of the memory die 66

(FIG. 4). In this manner, they can be loaded while the FPGA 68 comprising logic cells 84 are in operation."). None of the challenged claims require loading the FPGA while it is in operation, which further undermines Patent Owner's position.

In sum, the '214 patent does not support Patent Owner's contentions regarding the wide configuration data port.[13] Additionally, Patent Owner's expert, Dr. Souri, describes a wide configuration data port as *interconnecting* "the two elements of a memory die and a programmable array die" rather than *being within* the memory array. Ex. 2011 ¶ 54. Moreover, Patent Owner appears elsewhere to describe the wide configuration data port as the "die-area interconnection arrangement with buffer cells," which further supports that the wide configuration data port is not a structure provided within the memory array. PO Sur-reply 2 ("the novel die-area interconnection arrangement with buffer cells (i.e., wide configuration data port) allows the parallel loading of data from the memory die to the programmable array that is responsible for the claimed acceleration").

Furthermore, the '214 patent consistently identifies acceleration with stacking techniques that include contacts throughout the stacked dies, without requiring other structure. For example, the abstract of the '214 patent describes a processor module "constructed by stacking one or more thinned

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[13] Moreover, during the Oral Hearing, Patent Owner's counsel allowed for buffer cells being on the FPGA. Specifically, Patent Owner's counsel argued that "when the buffer cells are on the FPGA, it then raises the question, okay, well, what's on the memory array, right. And my answer would be probably more buffer cells." Tr. 54:21–24.

microprocessor, memory and/or . . . FPGA die elements and interconnecting the same utilizing contacts that traverse the thickness of the die." Ex. 1001, code (57). The abstract indicates that this processor module "allows for significant acceleration of the sharing of data between the microprocessor and the FPGA element. . . ." Ex. 1001, code (57). Notably, this description of "significant acceleration" does not include a wide configuration data port or buffer cells.

Additionally, the '214 patent similarly describes stacking techniques as accelerating the sharing of data between the microprocessor and the FPGA and accelerating external memory references, without referring to a wide configuration data port or buffer cells. *See* Ex. 1001, 2:64–66 (describing "a processor module with a reconfigurable capability that may include, for example, a microprocessor, memory and FPGA die stacked in a single block for the purpose of accelerating the sharing of data between the microprocessor and FPGA"), 2:64–66 (indicating "the FPGA module may employ stacking techniques to combine it with a memory die for the purpose of accelerating external memory references"). The '214 patent indicates that "[b]ecause the various die 64, 66 and 68 (FIG. 4) have very short electrical paths between them, the signal levels can be reduced while at the same time the interconnect clock speeds can be increased." Ex. 1001, 5:50–53 (emphasis added). Similarly, "there is an added benefit of . . . increased operational bandwidth." Ex. 1001, 5:48–50. Notably, the descriptions of shorter electrical paths, increased speed and bandwidth are due to the stacking techniques and are made within the context of Figure 4 without mention of Figure 5's wide configuration data port and buffer cell embodiment. As noted above,

even reconfiguration may occur without the specific wide configuration data port embodiment of Figure 5, for example, "[o]ther methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68." Ex. 1001, 5:41–45.

For these reasons, we conclude that the claims do not require a wide configuration data port (with or without buffer cells) *within a memory array* under the ordinary and customary meaning or otherwise.

D. *Asserted Obviousness of Claims 1, 2, 4, 6, 26, 27, 29, and 31*

Petitioner contends the subject matter of claims 1, 2, 4, 6, 26, 27, 29, and 31 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 1, 14–38. Patent Owner disputes Petitioner's contentions. PO Resp. 18–39.

1. *Summaries of Zavracky, Chiricescu, and Akasaka*

a. Disclosure of Zavracky

Zavracky describes "a multi-layered structure" including a "microprocessor . . . configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure." Ex. 1003, code (57). Zavracky's "invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing." *Id. at* 2:5–10. Zavracky includes numerous types of stacked elements,

including "programmable logic devices" stacked with "memory" and "microprocessors." *See id.* at 5:19–23.

Zavracky's Figure 12 follows:

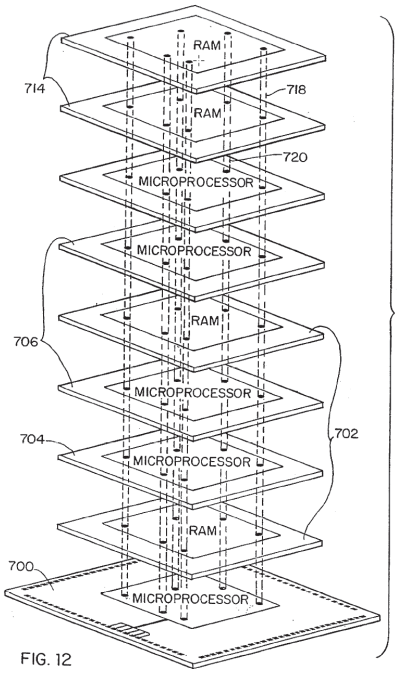

Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements wherein "buses run vertically through the stack by the use of inter-layer connectors." Ex. 1003, 12:24–26.

b. Disclosure of Chiricescu

Chiricescu describes a three-dimensional chip, comprising an FPGA, memory and routing layers. Ex. 1004, 232. Chiricescu's FPGA includes a "layer of on-chip random access memory . . . to store configuration information." *Id.* Chiricescu describes and cites the

published patent application that corresponds to Zavracky as follows:

> At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip [3].

See Ex. 1004,232, 235 (citing "[3] P. Zavracky, M. Zavracky, D-P Vu, and B. Dingle, '*Three Dimensional Processor using Transferred Thin Film Circuits*,' US Patent Application # 08-531-177, allowed January 8, 1997").[14]

Chiricescu describes "[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information." Ex. 1004, 232. Chiricescu also describes using memory on-chip to "significantly improve[] the reconfiguration time," explaining as follows:

> The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to manage cache memory can be used to administer the configuration data.

Id. at 234.

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[14] Zavracky lists the same four inventors and "Appl. No. 531,177," which corresponds to the application number cited by Chiricescu.

Figure 2 of Chiricescu follows:

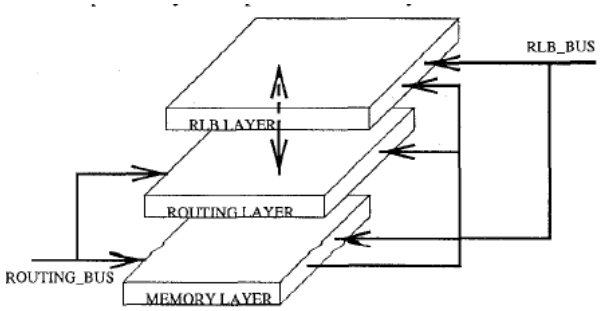

Figure 2. The layers of our 3-D FPGA architecture.

Figure 2 illustrates three layers in the 3D-FPGA architecture, with the RLB layer including routing and logic blocks in a "sea-of-gates FPGA architecture," a routing layer, and the memory layer (to program the FPGA). *See* Ex. 1004, 232–33.

c. Disclosure of Akasaka

Akasaka generally describes trends in three-dimensional integrated stacked active layers. Ex. 1005, 1703.[15] Akasaka states that "tens of thousands of via holes" allow for parallel processing in stacked 3-D chips, and the "via holes in 3-D ICs" decrease the interconnection length between IC die elements so that "the signal processing speed of the system will be greatly improved." Ex. 1005, 1705. Akasaka further explains that "high- speed performance is associated with shorter interconnection delay time and parallel

[15] Petitioner refers to pages in Ex. 1005 using the page numbers in the original article (e.g., 1703–1714) rather than the page numbers of the exhibit itself (e.g., 1–23). For convenience we follow Petitioner's practice of citing the page numbers of the original article.

processing" so that "twice the operating speed is possible in the best case of 3-D ICs." Ex. 1005,1705.

Also, Akasaka discloses that "input and output circuits . . . consume high electrical power." Ex. 1005, 1705. However, "a 10-layer 3-D IC needs only one set of I/O circuits," so "power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs." Ex. 1005, 1705.

Figure 4 of Akasaka follows:

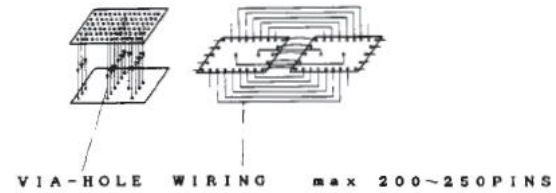

Fig. 4. Wiring for parallel processing in 2-D and 3-D ICs.

Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

2. *Petitioner's Combination of Zavracky, Chiricescu, and Akasaka*

Before proceeding through a detailed analysis of Petitioner's and Patent Owner's respective arguments and evidence, we provide some general analysis regarding the limitations of the independent claims to provide context for our detailed analysis.

a. General Contentions Regarding Independent Claim Limitations

In the main, Petitioner relies on Zavracky's disclosure of a stack of functional circuit elements, including microprocessor and memory elements through which "buses run vertically through the stack

by the use of inter- layer connectors." Ex. 1003, 12:24–26. Petitioner points to Zavracky's Figures 12 and 13 as disclosing a PLD (programmable logic device) and memory array in the stack as the recited first and second integrated circuit functional elements and the inter-layer connections (described as "via holes" or "contact holes") as the electrical coupling between the elements. Pet. 23–28 (citing, e.g., Ex. 1003, 9:45–45. 12:28–38, 2:1-7, 2:2–6, 5:19–23, 12:12–38, 6:48–50; 5:21–23, 12:33–36, Figs. 12, 13).

With regard to the recited FPGA, Petitioner provides evidence that one of ordinary skill in the art would understand that the PLD 802 at the bottom layer of the stack shown in Figure 13 was a field programmable gate array (FPGA) because a PLD was a type of FPGA. Pet. 24 (citing Ex. 1035, 1:29–30 (stating "a field programmable gate array (FPGA) 100, which is one type of PLD"); Ex. 1037, 1:13–22 (indicating "[o]ne type of PLD, the field programmable gate array (FPGA); Ex. 1038, Abstract (indicating a "programmable logic device (PLD), such as a field programmable gate array (FPGA)"). Petitioner also provides evidence that Zavracky's programmable logic array (also called programmable logic device) 802 is programmable to provide a user-defined communication protocol and, as such, functions as a processing element, as required by the claims. Pet. 28 (citing Ex. 1002 ¶ 302 (citing Ex. 1003, 12:28–38; Ex. 1057, 57; Ex. 1040, 319)).

Petitioner relies on Chiricescu in its combination of Zavracky, Chiricescu, and Akasaka for teaching a memory layer to which configuration data from "off-chip memory" is loaded and from which Chiricescu's FPGA can be reconfigured with that reconfiguration

data. Pet. 29–30 (citing Ex. 1004, 232, 234; Ex. 1002 ¶¶ 304–07). Petitioner contends that Chiricescu's memory layer accelerates reconfiguration of Chiricescu's FPGA because reconfiguration data that has already been loaded into the memory array is used to reconfigure the FPGA. Pet. 30. In this way, as Petitioner indicates, Chiricescu addresses the "main bottleneck in the implementation of a high performance configurable computer machine [which] is the high configuration time of an FPGA." Ex. 1004, 232; *see* Pet. 29–30 (quoting ex. 1004, 232; citing Ex. 1002 ¶ 304–07).

As Petitioner indicates, Chiricescu describes "[t]he architecture of a 3- dimensional FPGA for reconfigurable computing machines" and this architecture "is based on a novel 3-D circuit technology developed at Northeastern University," referring to Zavracky. Ex. 1004, 232 (Abstract), 235 n.3; Pet. Reply 13. Chiricescu specifically notes "[a]t Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip" and cites Zavracky for this technology. Ex. 1004, 232, 235 n.3.

Petitioner relies on Chiricescu to bolster Petitioner's position relying on Zavracky for teaching or suggesting a programmable FPGA. Specifically, Petitioner relies on Chiricescu's disclosure that one of its "key features" is "quickly reconfigur[ing]" its FPGA as a processing element to implement "arbitrary logic." Petitioner provides evidence in the form of credible testimony by Dr. Franzon that Chiricescu

shows reconfiguring an FPGA to perform multiplication. Pet. 29 (citing Ex. 1002 ¶ 303 (describing Ex. 1004, 234 ("FPGA is reconfigured from performing AxB to AxC or vice versa") as providing an example of "the multiplication of a 4-bit variable")).

Independent claim 2 additionally requires that the number of contact points (that electrically couple the first and second integrated circuit functional elements) be "distributed throughout the surfaces of said functional elements." For this limitation, Petitioner relies on Zavracky's express teaching that "openings or via holes" used for inter-layer connections "can be placed anywhere on the die" of various functional elements, such that the connections "are not limited to placement on the outer periphery." Pet. 32 (quoting Ex. 1003, 6:43–47, 13:43–46, 14:56–63). Petitioner bolsters its position by further relying on Akasaka's disclosure of electrical coupling active layers in 3-D integrated circuits through "via holes" as shown in Akasaka's Figure 4 and Akasaka's statement that "[s]everal thousands or several tens of thousands of via holes are present in these devices." Pet. 32 (quoting Ex. 1005, 1705).

In addition to contesting Petitioner's reasons to combine the references, Patent Owner contests the "memory array functional to accelerate" limitations in each independent claim. Patent Owner throughout its briefing combines specific contentions with Petitioner's contentions regarding "the memory array functional to accelerate" limitations with Patent Owner's overly narrow interpretation—that the claims require a wide configuration data port as Patent Owner interprets Figure 5 of the '214 patent to be and/or that the claims require buffer cells to be

present in the wide configuration data port. For the reasons discussed previously in Section II.C (Claim Construction), we do not agree with Patent Owner's position and so do not agree with Patent Owner's many arguments that incorporate Patent Owner's improperly narrow reading of the claims.

Many of Patent Owner's arguments also apply to a misunderstanding of Petitioner's combination. For example, Patent Owner seems unduly focus on Chiricescu's data transfer when loading configuration data *into the memory cells*, whereas Petitioner's combination relies on acceleration of reconfiguring the FPGA using configuration data that *has been* loaded into Chiricescu's memory layer. Patent Owner's arguments such as these that do not address Petitioner's combination do not undermine Petitioner's combination.

Patent Owner also at times asserts that Dr. Franzon "admitted" something during his deposition testimony. As described below with respect to specific instances, we do not agree with Patent Owner's characterization where Patent Owner's arguments overgeneralize Dr. Franzon's testimony and do not sufficiently take into consideration the context of Dr. Franzon's testimony. For example, Patent Owner characterized Dr. Franzon's testimony discussing a prior art reference (Trimberger)[16] as "unequivocally stat[ing] that Petitioner's proposed combination was not feasible" and "admitting Chiricescu's 'RLB BUS' that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the

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[16] Ex. 1006 (Trimberger) has not been asserted in any of Petitioner's grounds in this proceeding.

'214 Patent." PO Sur-reply 14 (citing Ex. 2012, 71:19–72:1; PO Resp. 29); PO Sur-reply 19–20 (citing Ex. 2012, 80:10–22). We address Patent Owner's challenges to Dr. Franzon's testimony in detail below.

We now turn to addressing Petitioner's contentions and Patent Owner's arguments in detail.

b. Petitioner's Reasons to Combine Zavracky, Chiricescu, and Akasaka

In contending the subject matter of claims 1, 2, 4, 6, 26, 27, 29, and 31 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka, Petitioner provides reasons that one of ordinary skill in the art would have "integrate[d] the disclosures of Zavracky (including a stacked interconnected programmable 3-D module), Chiricescu (including accelerated FPGA reconfiguration using stacked memory), and Akasaka (including thousands of distributed interconnections)." Pet. 18; *see* Pet. 18– 19 (citing Ex. 1002 ¶¶ 221–28 (citing Ex. 1004, 234; Ex. 1003, 5:65–66; Ex. 1020, 2; Ex. 1055 [0014]; Ex. 1040, 317)); Pet. 18–22 (discussing integrating Zavracky with Chiricescu and integrating Akasaka with Zavracky and Chiricescu). Petitioner also includes reasons one of ordinary skill in the art would have had a reasonable expectation of success. See Pet. 18–22; Pet. 20 ("With these understandings, [one of ordinary skill in the art] would have had a reasonable expectation of success in achieving the Zavracky-Chiricescu combination."); Pet. 20–21 (One of ordinary skill in the art "would have expected success in the combination [] by knowing of successful similar prior art designs.").

(i) *"[F]olding in" Chiricescu's teachings (including using stacked memory to reconfigure the FPGA) with Zavracky's 3D stacks*

Relying on Dr. Franzon's testimony, Petitioner contends that one of ordinary skill in the art would have "been encouraged to fold in Chiricescu's teachings (including using stacked memory to reconfigure the FPGA) with Zavracky's 3D stacks, understanding that it would lead to 'significant[] improvement in the reconfiguration time." Pet. 18–19 (citing Ex. 1002 ¶ 212); Ex. 1002 ¶ 212 (quoting Ex. 1004, 234 ("The elimination of loading configuration data on an as needed basis from memory off-chip significant improves the reconfiguration time for an on-going application."), ¶ 217 (testifying one of ordinary skill in the art "would readily recognize (because a cache is a building block of computer devices, and used in almost every processor on Earth) the ability to accelerate externa memory references by 'eliminat[ing] loading configuration data on an as needed basis' would, as Chiricescu teaches, 'significant improves the reconfiguration time for an on- going application.'"). Petitioner points out that "Chiricescu, for example, explicitly references and uses the interconnections of Zavracky, as detailed in § VII.A.2" as another reason one of ordinary skill in the art would have folded in Chiricescu's teaching with Zavracky's 3D stacks. Pet. 18 (noting the explicit citation to and description of Zavracky in Chiricescu); Ex. 1002 ¶ 218 (explaining that (i) Chiricescu and the Zavracky inventors were in the same research group at a university and (ii) "Chiricescu describes and cites the Zavracky patent application in his paper on the first page" (citing Ex. 1004, 232)).

Based on Dr. Franzon's declaration testimony, Petitioner also asserts that one of ordinary skill would have enhanced and expanded Zavracky's programmable logic device within its co-stacked microprocessors and memories to include image and signal processing tasks as Chiricescu suggests by teaching the use of FPGAs to implement arbitrary logic functions. Pet. 19 (citing Ex. 1002 ¶¶ 229–30; Ex. 1005, 1705; Ex. 1003, 12:25–30; Ex. 1004, 232; Ex. 1058, 41; Ex. 1048); Ex. 1002 ¶ 229 (Dr. Franzon's testifying that image and signal processing were recognized as good applications for 3-D stacked chips that required parallel computation, such as signal processing citing various references for support (including Ex. 1005, 1705; Ex. 1048; Ex. 1003, 12:25–30; Ex. 1004, 232; Ex. 1058, 41)).

Relying on Dr. Franzon's declaration testimony, Petitioner contends that one of ordinary skill in the art would have had a reasonable expectation of success in making this combination because one of ordinary skill in the art "would have viewed Chiricescu with Zavracky as a routine modification." Pet. 20 (Ex. 1002 ¶¶ 231–32). Dr. Franzon's opinion that the combination was a routine modification is supported by Dr. Franzon's credible explanation that "Chiricescu would have actually just be[en] providing what Zavracky is generally describing when Zavracky states that in Figure 13, its programmable logic device 'can be programmed to provide for user-defined communication protocol[s].'" Ex. 1002 ¶ 231.

Again relying on Dr. Franzon's declaration testimony, Petitioner also contends that one of ordinary skill in the art "would have been familiar with other prior art processor modules including other

microprocessor-FPGA- memory combinations." Pet. 20 (Ex. 1002 ¶¶ 231–32 (citing Ex. 1026)). Dr. Franzon's well-reasoned testimony is supported by evidence in the form of a reference "that performs exactly that stack" that was described in Dr. Franzon's declaration testimony regarding background art known to one of ordinary skill in the art. Ex. 1002 ¶ 232 (citing Ex. 1026; referring to Ex. 1002 ¶¶ 125–28).

(ii) *Applying Akasaka's Thousands of Distributed Contact Points*

Relying on Dr. Franzon's declaration testimony, Petitioner also contends that it was "a predictable advantage and also suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity." Pet. 20 (citing Ex. 1002 ¶ 233; Ex. 1005, 1705). Petitioner adds that "Zavracky and Chiricescu . . . invited such a combination." Pet. 20 (citing Ex. 1003, 6:43– 47 ("connections . . . can be placed anywhere on the die"); Ex. 1004, 232 (similar); Ex. 1020, 9). Petitioner further relies on Dr. Franzon's testimony as follows:

> [One of ordinary skill in the art] knew of the need for replicated "common data memory" in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence. Ex. 1002 ¶ 236 (citing Ex. 1034, 466–469; Ex. 1005, 1713 & Fig. 25). That structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky. Ex. 1002 ¶ 237. [One of ordinary skill in the art] thus would have been motivated to seek out Akasaka's distributed

> contact points in order to build a "common data memory." The POSITA's background knowledge, including prior art successes, would have suggested success in this combination. *Id.* (citing Ex. 1005, Ex. 1021).

Pet. 21.

In his declaration testimony cited by Petitioner, Dr. Franzon further explains that the common data memory "still obtain[s] the speed and cost advantages of having an FPGA-based stack (e.g., the FPGA being faster than the software running on a microprocessor, and cheaper than an ASIC)." Ex. 1002 ¶ 237. Dr. Franzon also explains that "the POSITA would have known that the more densely connected communication structure of Akasaka would enable desirable uses of the Zavracky-Chiricescu 3D chip stack," including multi-processor cache coherence. Ex. 1002 ¶ 236 (citing Ex. 1713, Fig. 25; Ex. 1034, 466–469).

Relying on Dr. Franzon's declaration testimony, Petitioner contends that one of ordinary skill in the art would have had an expectation of success in making this combination because one of ordinary skill in the art "would have known many references teaching stacked functional-element dies with thousands of distributed connections, including" depicted stacks (e.g., Figure 4 in Exhibit 1020, Figure 9 in Exhibit 1028, and Figure 1(a) in Ex. 1021). Pet. 21 (referring to Pet. 8–10).

c. Patent Owner's Contentions

Patent Owner contends that Petitioner fails to provide the required articulated reasoning to support

a conclusion of obviousness. PO Resp. 2–3, 23–39; PO Sur-reply 10–14.

(i) Alleged Misrepresentation of Chiricescu

First, Patent Owner contends that "Petitioner misrepresents Chiricescu to allege motivation to combine Zavracky and Chiricescu." PO Resp. 24–25 (Section VI.A.3(a)). Patent Owner specifically asserts that Chiricescu does not employ Zavracky's principles, does not utilize Zavracky's principles to improve reconfiguration time, and "does not employ Zavracky's die-area vertical interconnections to connect a memory die to an FPGA, and no die- area vertical is involved whatsoever in reconfiguring Chiricescu's FPGA." PO Resp. 24 (citing Pet. 18–19, Ex. 1004, 232 (Exhibit page 1), 234 (Exhibit page 3); Ex. 2011 ¶ 61[17]).

The record does not support this line of argument. Chiricescu's Abstract indicates the paper describes "[t]he architecture of a 3-dimensional FPGA for reconfigurable computing machines" and "is based on a novel 3-D circuit technology developed at Northeastern University." Ex. 1004, 232 (Abstract); *see* Pet. Reply 13. Chiricescu specifically notes "[a]t Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer

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[17] Dr. Souri's declaration testimony cited by Patent Owner (Ex. 2011 ¶ 61) is a single-sentence conclusion that provides no more reasoning than that included in the Patent Owner Response to the Petition (Paper 19).

vias) placed anywhere on the chip" and citing Zavracky for this technology. Ex. 1004, 232, 235 n.3.

Moreover, Patent Owner unduly focuses on Chiricescu's use of 'on- chip' memory to mitigate the time it takes to transfer configuration data from 'off-chip'" and contends that Petitioner's combination does not "mak[e] any use of Zavracky's die-area vertical interconnections to transfer configuration data from the 'on-chip' memory into the FPGA." PO Resp. 24 (citing Ex. 1004, 232, 234). Patent Owner also argues that "[n]either Zavracky nor Chiricescu even contemplate using die-area inter-layer vertical interconnections to move data between a programmable array and a memory, such as is recited in Claims 1, 2, 26, and 27." PO Resp. 24 (citing Ex. 2011 ¶ 62); Ex. 2011 ¶ 62 (Dr. Souri's conclusory testimony that contains no more reasoning than in the Patent Owner's Response).

The record does not support this line of argument. First, Petitioner's combination focuses on Chiricescu for "using stacked memory to reconfigure the FPGA" (Pet. 18–19 (citing Ex. 1004, 232)). For example, Chiricescu discloses using 3-D layered FPGAs with interlayer vias and describes 3-D hierarchical interconnections between logic blocks as a feature. *See* Chiricescu, 232 ("Our architecture utilizes an extremely flexible 3-D hierarchical connection scheme in which the interconnections between logic blocks do not affect the use of logic resources. Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.").

As discussed above, Zavracky's Figure 13 shows that Zavracky contemplates moving data on vertical

buses between RAM memory 808 (and RAM memory on processor layer 806) and programmable array 802 (Ex. 1003, 12:29–39), and Chiricescu's Figure 2 shows that Chiricescu contemplates moving data on "vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip" (based on Chiricescu's characterization of Zavracky) between memory layer and the "sea of gates FPGA" RLB layer (Ex. 1004, 232); *see also* Ex. 1004, 232 § 1 ("Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.").

Also, Petitioner shows persuasively one of ordinary skill in the art would have recognized that speed improvement emanates partly from shorter interconnection distances and/or parallel processing using a larger number of vias (as compared to connections on the same plane). *See* Reply 6 (arguing Zavracky's "approach **accelerates** communication between the dies in the chip by way of '**smaller delays** and **higher speed** circuit performance'" (emphasis by Petitioner (quoting Ex. 1003, 3:4–14)), and arguing that "Zavracky's short interior 'inter-layer connectors' to stacked 'random access memory . . . results in reduced memory access time, **increasing the speed** of the entire system.' (emphasis by Petitioner (quoting Ex. 1003, 11:63–12:2)).

Nor do we agree with Patent Owner's contention that, "because Chiricescu discloses that the configuration data is stored in on-chip memory, the approach of Zavracky-Chiricescu would result in a structure in which data is removed from the microprocessor cache and placed in the FPGA's on-

chip memory, making it **much harder** for the microprocessor to access memory given that the same type of slow front side bus distinguished in the '214 Patent would be required for the microprocessor to access the FPGA's on-chip memory, [which would] result in significantly **decreased** processing speeds . . ., thus not leading to an improvement in the reconfiguration time." PO Resp. 24–25 (citing Ex. 2011 ¶ 63) (emphasis in PO Resp.); Ex. 2011 ¶ 63 (Dr. Souri's testimony contains no additional reasoning than that in the Patent Owner's Response). Petitioner's combination "folding in" Chiricescu's teaching does not require configuration data to be stored in on- chip memory, and so Patent Owner's contentions do not address Petitioner's combination.

Moreover, neither Petitioner nor Dr. Souri sufficiently consider Petitioner's more general showing, based on Dr. Franzon's declaration testimony, that one of ordinary skill in the art "would have recognized that the more densely connected communication structure of Akasaka would enable desirable uses of the Zavracky-Chiricescu 3D chip stack." Pet. 21 (citing Ex. 1002 ¶ 236 (citing Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25)).

On balance, we find Dr. Franzon's testimony in this regard more credible than Dr. Souri's testimony. Dr. Franzon's testimony is based on specific descriptions of references consistent with his opinion, whereas Dr. Souri's testimony does not provide evidentiary support.

For these reasons, we do not agree with Patent Owner's position that Petitioner "misrepresents Chiricescu" and so does not provide articulated reasoning to support a conclusion of obviousness.

(ii) Motivation Alleged to Be Untethered to Claims

Second, Patent Owner also contends that Petitioner's alleged motivation to combine Zavracky and Chiricescu "is untethered to the challenged claims."[18] PO Resp. 25–26 (Section VI.A.3(b)). Patent Owner specifically argues that Petitioner does not provide motivation to combine Zavracky and Chiricescu "to reach a memory array functional to accelerate an external memory reference[] or accelerate the reconfiguration of a programmable array, as claimed." PO Resp. 25–26 (citing Ex. 2011 ¶ 64).

The record does not support this line of argument. Petitioner tethers its argued reasons to combine to accelerating external memory references and reconfiguration of a programmable array. For example, Petitioner asserted that one of ordinary skill would have combined "Chiricescu's teachings (including using stacked memory to reconfigure the FPGA) with Zavracky's 3D stacks, understanding that it would lead to 'significant[] improvement in reconfiguration time." Pet. 18 (citing Ex. 1002 ¶¶ 221–28 (citing Ex. 1004, 234; Ex. 1003, 5:65–660; Ex. 1020, 2; Ex. 1055 [0014]; Ex. 1040, 317)); Pet. Reply 14 (citing Pet. 18). Similarly, Chiricescu's technology that acts like cache memory for reconfiguration data results in accelerated access to external memory references (Pet. 30) likewise is tethered to the claimed acceleration provided by Chiricescu's technology to

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[18] We understand Patent Owner's "untethered" argument to challenge Petitioner's showing as to why "a skilled artisan would have had reason to combine the teaching of the prior art references to achieve the claimed invention." *PAR Pharm.*, 773 F.3d at 1193.

reconfigure the FPGA. Pet. 18–19; *see* Pet. Reply 14–15.

In addition, Petitioner discusses in the context of the programmability of an FPGA recited in each of the challenged claims. As such, and in contrast to Patent Owner's assertion that "Petitioner fails to articulate any reason that Chiricescu's alleged teaching of performing 'arbitrary logic functions' is related to the claimed invention," (PO Resp. 26), Petitioner tethers the description one of Chiricescu's "'key features' is that its FPGA can be 'quickly reconfigured' to implement 'arbitrary logic'" to the recited limitation that "said field programmable gate array is programmable as a processing element." Pet. 28–29. Thus, Petitioner's position that one of ordinary skill in the art "would have taken Chiricescu's suggestion of a FPGA to perform 'arbitrary logic functions'" as a reason to combine the references is tethered to claim language. *See* Pet. 19.

(iii) Alleged Major Modifications

Third, Patent Owner contends that Petitioner's alleged motivation to combine Zavracky and Chiricescu "requires major modifications." PO Resp. 26–29 (Section VI.A.3(c)). Patent Owner argues that Chiricescu's narrow data port, the lack "of the type of wide configuration data port responsible for the accelerating features of the challenged claims," "or to arrange a microprocessor and programmable array such that the two components share data" would necessitate major modifications beyond the level of ordinary skill and neither Zavracky or Chiricescu discloses a structure—"a memory array that achieves the claimed acceleration (i.e. utilizing a portion of the wide configuration data port)" in the '214 patent—to

address the problem of reducing the amount of time to move data from a memory die to the programmable array. PO Resp. 28 (citing Ex. 2011 ¶ 68). Dr. Souri explains that the major modification to configure a stacked module to meet the acceleration limitations of the claims requires a "wide configuration data port between the memory and the FPGA" and that such a modification would alter Chiricescu's principle operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB Bus and its 'routing layer,' which Chiricescu declares 'is of critical importance since it is used for the implementation of the interconnection of the non-neighboring RLBs.'" Ex. 2011 ¶ 67 (citing Ex. 1004, 233 (page 2 of exhibit); *see* PO Resp. 27.

As discussed previously (in Section II.C), however, the '214 patent in Figure 5 does not support Patent Owner's contentions that the claims require such a structure *within* the memory array. *See, e.g.,* PO Resp. 19. The '214 patent describes the vertical contacts distributed throughout the surface ("vias") to allow multiple short paths for data transfer between the memory and processing element. As Petitioner also persuasively argues, no "'modifications' are required to Chiricescu at all because the Petition's combination involves 'fold[ing] in Chiricescu's teachings (including using stacked memory to reconfigure[] the FPGA) with Zavracky's 3D stacks." Pet. Reply 15 (quoting Pet. 17–18).

Moreover, even if employing Chiricescu's FPGA structure also suggests implementing its routing layer on a separate layer, Chricescu does not describe its routing layer as a narrow port, contrary to Patent

Owner's arguments. Pet. Reply 15–16 (noting that Dr. Franzon did not admit Chiricescu includes a narrow port and citing Dr. Franzon's testimony that on-chip area-wide connections in 3D stacks were well-known (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68; Ex. 1020)); *see also* Ex. 1004, 232, Fig. 2 (depicting connections between the memory layer, routing layer, and RLB layer (a "sea-of-gates FGPA structure") with connections that are distinct from the RLB bus); Ex. 1004, 232 (noting that "routing congestion will also be improved by the separation of layers," further suggesting that the routing layer is not part of a narrow port). In addition, Petitioner indicates that "Chiricescu describes 'vertical metal interconnections (i.e., interlayer vias),' and '**three separate layers with metal interconnects between them**.'" Pet. Reply 13 (citing Ex. 1004, 232). Ciricescu's "architecture is based on technology developed by Zavracky at Northeastern University." Pet. Reply 13 (quoting Ex. 1004, 232). And Ciricescu states that Zavracky's architecture provides "3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) *placed anywhere* on the chip." Ex. 1004, 232 (emphasis added). For these reasons, the record does not support a conclusion that Chricescu's principle of operation does not require a narrow port, contrary to Patent Owner's arguments.

(iv) *Akasaka and Common Data Memory*

Fourth, Patent Owner further contends that "Akasaka exacerbates the problems with Petitioner's obviousness combination." PO Resp. 29–33 (Section VI.A.3(d)). According to Patent Owner, "Akasaka's only relevant disclosure is the 'common data memory' concept involved in the Petition, which does not

disclose data shared between any processors" but "discloses that each processor in the stack accesses only the memory *in its own layer*." PO Resp. 30 (citing Ex. 1005, 11, Fig. 11; Ex. 2011 ¶ 71).

The record does not support this line of argument. Petitioner's combination relies on Akasaka for teaching "thousands of distributed interconnections." Pet. 18; *see also* Pet. 17–18 (overview of Akasaka). Petitioner uses Akasaka's common data layer to provide a reason that one of ordinary skill in the art would have used Akasaka's "thousands of distributed interconnections" in Petitioner's combination of Zavracky-Chiricescu that includes Zavracky's three-dimensional circuits electrically connected by via holes. Pet. 21; *see, e.g.,* Pet. 26–27 (citing Ex. 1003, 14:51–63, Figs. 12–13).

More specifically, relying on Dr. Franzon's declaration testimony, Petitioner contends that one of ordinary skill in the art would have known "of the need for replicated 'common data memory' in stacked designs, including as taught in Akasaka, to enable, e.g., multiprocessor cache coherence." Pet. 21 (citing Ex. 1002 ¶ 236 (citing Ex. 1034, 466–69; Ex. 1005, 1713, Fig. 25)).

Dr. Franzon explains that particular technique ("Write Broadcast") ensures multi-processor cache coherency by "broadcast[ing] the new data over the bus [so that] all copies are updated with the new value." Ex. 1002 ¶ 236 (citing Ex. 1034, 466–69 (computer architecture text book)). Dr. Franzon relates this known technique for ensuring multi-processor cache coherency to keeping replicated 'common data memory' in stacked designs consistent. Dr. Franzon points to Akasaka's Figure 25 as

illustrating such a broadcast technique to keep the memory data in each independent layer consistent. Ex. 1002 ¶ 236 (discussing Ex. 1005, Fig. 25, 1713). Dr. Franzon further explains that Akasaka's Figure 25 structure implementing the broadcast technique "would be difficult in the design to accomplish with just a limited number of interconnections between dies n Zavracky and certainly would be improved by Akasaka's distributed connections teaching." Ex. 1002 ¶ 237. This explanation supports Dr. Franzon's opinion that one of ordinary skill in the art "would have been motivated to seek out Akasaka's distributed contact points in order to build a 'common data memory,' as taught in Akasaka, while still obtaining the speed and cost advantages of having an FPGA-based stack (e.g., the FPGA being faster than the software running on the microprocessor, and cheaper than an ASIC." Ex. 1002 ¶ 237.

As such, Dr. Franzon's explanation of broadcast techniques to enable 'common data memory' consistency provides a reason that one of ordinary skill in the art would include Akasaka's thousands of distributed interconnections (not just the smaller number taught by Zavracky) in Petitioner's combination of Zavracky, Chiricescu, and Akasaka. We do not understand Petitioner's position to require bodily incorporation of Akasaka's Figure 25 into Petitioner's Zavracky-Chiricescu combination, as Patent Owner seems to suggest. "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012). "What matters in the § 103 nonobviousness determination is whether a person of ordinary skill in the art, having

all the teachings of the references before him, is able to produce the structure defined by the claim." *Orthopedic Equip. Co., Inc. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983). Rather, we understand Petitioner's position to be that one of ordinary skill in the art would included Akasaka's thousands of distributed interconnections, motivated in part by Akasaka's Figure 25 illustration of keeping a common data memory consistent by parallel transfer of data.

Furthermore, Petitioner relies on Dr. Franzon's testimony that accomplishing the "common data memory" desirable for "multi-processor cache coherence" "would be more difficult to accomplish with a limited number of interconnections as in Zavracky." Pet. 21 (citing Ex. 1002

¶ 237).

For these reasons, we do not agree with Patent Owner's arguments that "Akasaka exacerbates the problems with Petitioner's obviousness combination." PO Resp. 29–33.

Moreover, Petitioner provides a second independent reason that one of ordinary skill in the art would had have to apply Akasaka's distributed contact points in the 3D stacks of Zavracky or Chiricescu. Petitioner points to advantages "suggested by Akasaka" that using Akasaka's distributed contact points "would increase bandwidth and processing speed through better parallelism and increased connectivity in the stack of Zavracky. Pet. 20 (citing Ex. 1002 ¶ 233 (quoting Ex. 1005, 1705); *see also* Pet. 17–18 (describing Akasaka's benefits). Petitioner relies on Dr. Franzon's declaration testimony that one of ordinary skill in the art would

have recognized these benefits and "would have sought out Akasaka's connectivity to improve Zavracky's stacks in applications requiring parallel processing," such as image processing. Pet. 20 (citing Ex. 1002 ¶¶ 233, 235; Ex. 1005, 1705, citing Ex. 1003, 6:43–47; Ex. 1004, 232, Ex. 1020, 9). We find Dr. Franzon's testimony in this regard to provide persuasive explanation and analysis that relies on quotations of specific passages that support his testimony. *See* Ex. 1002 ¶ 233 (explaining two reasons one of ordinary skill in the art would have combined Akasaka's distributed contact points with Petitioner's combination of Zavracky-Chiricescu: "increased parallelism (e.g., the ability . . . to move and process data simultaneously) and increased connectivity (e.g., the ability to access various parts of the chip directly"); quoting Ex. 1005, 1705 (Akasaka identifying benefits); reproducing Ex. 1005, Fig. 4 (titled "Wiring for parallel processing in 2-D and 3-D ICs and depicting "via-hole wiring").

(v) *Alleged Lack of Reasonable Expectation of Success*

Fifth, Patent Owner contends that "Petitioner fails to demonstrate how [one of ordinary skill in the art] would have integrated Akasaka's thousands of via interconnects with Zavracky-Chiricescu's design and circuitry with a reasonable expectation of success." PO Resp. 33 (Section VI.A.3(e)).

Regarding Patent Owner's arguments, first, we do not agree with Patent Owner's characterization of Dr. Franzon and Petitioner's analysis that one of ordinary skill in the art "would have understood the references *could be* combined" and, as such, fail to provide the requisite articulate reason to support a

conclusion of obviousness. PO Resp. 36. Rather, Petitioner and Dr. Franzon provides specific reasons why one of ordinary skill in the art *would have* combined the references in the manner proposed by Petitioner. *See* Pet. 18–22 (repeatedly stating "would have been motivated"; "would have been encouraged to"; "would have taken"; "would have recognized"); *see also* Pet. Reply 17 (Petitioner indicating that it did not make a "could be combined" argument).

Turning back to Patent Owner's assertion that Petitioner fails to demonstrate that one of ordinary *skill* in the art would have a reasonable expectation of success to integrate Akasaka's thousands of via interconnects with Petitioner's combination of Zavracky-Chiricescu (PO Resp. 33–34) and Patent Owner's contention that Petitioner "failed to 'account for a single one of [the alleged] problems' related to TSV (through-silicon vias) interconnections." Petitioner characterizes these issues as "at most normal engineering issues, not problems preventing a combination." Pet. Reply 17 (alteration in Reply). We note, as discussed above, that Petitioner relies on Dr. Franzon's testimony that accomplishing the "common data memory" desirable for "multi-processor cache coherence" "would be more difficult to accomplish with a limited number of interconnections as in Zavracky" than in using Akasaka's thousands of via interconnects. Pet. 21 (citing Ex. 1002

¶ 237).

Furthermore, Petitioner relies on Dr. Franzon's testimony that one of ordinary skill in the art's "background knowledge, *including* prior art successes, would have suggested success in this combination." Pet. 21 (citing Ex. 1002 ¶ 237 (citing Ex.

1005, Ex. 1021, 18)). In addition to Akasaka's description, Dr. Franzon identifies a 1998 IEEE article that, according to Dr. Franzon, describes a "large number of interconnects to SRAMs and DRAMs. Ex. 1002 ¶ 237 (citing Ex. 1021, 18 as "describing the large number of interconnects to SRAMs and DRAMs"). We credit Dr. Franzon's testimony based on additional evidence of what one of ordinary skill in the art would understand. We also note that generally it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) ("A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse."). Here the level of ordinary skill is a Bachelor's Degree in Electrical Engineering, with at least two years of industry experience. This further supports that one of ordinary skill in the art would have an expectation of success based on prior art successes of implementing a large number of interconnects to connect well-known circuits together such as FPGAs, microprocessor, and memories.

Additionally, many of Patent Owner's arguments seem to suggest bodily incorporation is required and must be explained for Petitioner to prevail. For example, Patent Owner asserts "Petitioner and Dr. Franzon's analysis wholly fails to provide any explanation whatsoever as to how Akasaka's thousands of via interconnections would be laid out, connected to, and operate with the various functional blocks of Zavracky-Chiricescu 3-D device circuitry, and therefore necessarily would work." PO Resp. 38. In another example, Patent Owner asserts that

> [a]t the time of the invention, a POSITA was aware of numerous TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ("HDL") algorithms, which must be considered. Souri Decl., ¶ 78; Ex. 2014 at 85, 87, 89.
>
> Petitioner's combination does not account for a single one of these problems, let alone demonstrate that they could have been solved by a POSITA at the time of the invention with a reasonable expectation of success.

PO Resp. 37.

To the extent that Patent Owner supports its position with a suggestion that bodily incorporation is required, we do not agree with such arguments by Patent Owner. "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012). "What matters in the § 103 nonobviousness determination is whether a person of ordinary skill in the art, having all the teachings of the references before him, is able to produce the structure defined by the claim."

Nor do we agree with Patent Owner's characterization of Dr. Franzon's testimony as "unequivocally stat[ing] that Petitioner's proposed combination was not feasible." PO Sur-reply 14 (citing Ex. 2012, 71:19–72:1; PO Resp. 29). Rather, Dr. Franzon's testimony indicated that *off-chip access* to a wide configuration data port 100,000 bits wide was not feasible. He testified

> one of ordinary skill in the art "would understand that you have an off-chip access to this wide configuration data port. That off-chip access can't be, for example, 100,000 bits wide. For practical reasons you can't have that number of IO. And this is both in the case of Trimberger and [the challenged patent], memory going from the external to the module.

Ex. 2012, 71:19–72:1.

This testimony relates to the previous discussion about using narrow ports to load configuration information, as in Chiricescu, and does not address the feasibility of using such pre-loaded configuration information to reconfigure a FPGA or accelerate external references to memory, both of which happen in the stack using the short vias that connect the layers in the stack. Here again, Patent Owner conflates the loading of the stack with configuration information with the claimed elements—including the memory array functional to accelerate reconfiguration of a FPGA as a processing element (independent claims 1 and 2) or the memory array functional to accelerate external memory references to said processing element (independent claims 26 and 27).

3. *Independent Claims 1, 2, 26, and 27*

Turning to the independent claims 1, 2, 26, and 27, Petitioner presents various arguments and evidences regarding the prior art purported teaching or suggesting the claimed elements. *See, e.g.,* Pet. 22–33, 36–38.

a. Undisputed Limitations of Independent Claims 1, 2, 26, and 27

Claim 1 recites "[a] programmable array module comprising" various elements. Petitioner contends that one of ordinary skill in the art would have understood Zavracky to be describing a programmable array module from Zavracky's disclosure of (i) "a common module body to perform a combined function," (ii) a module based on "programmable logic array 802," and (iii) its invention as relating to "the structure [of] vertically stacked and interconnected circuit elements for. . . programmable computing." *See* Pet. 22 (relying on Ex. 1003, 9:42–45, 12:28–38, 2:1–7, Fig. 13; citing Ex. 1002 ¶¶ 282–86). Petitioner further argues that the combination of Zavracky and Chiricescu's "system where the focus of the 3D module is on a FPGA and a memory designed to accelerate external references . . . to the FPGA" "provid[es] a programmable array module," relying on FPGA as a programmable array. Pet. 22–23 (citing Ex. 1004, 234).

Petitioner contends that Zavracky discloses "at least a first integrated circuit functional element including a field programmable gate array" (limitation [1.1]). Pet. 23–26. Petitioner relies on Zavracky's Figure 12 as disclosing "layers that comprise integrated circuit functional elements" that perform specific functions, including being a memory or microprocessor. Pet. 23 (citing Ex. 1003, 2:2–6, 5:19–23, Fig. 12). Petitioner further relies on Zavracky's Figure 13 as disclosing an integrated circuit element that functions as a programmable logic device. Pet. 23.

For the recited "field programmable gate array" (FPGA), Petitioner relies on Zavracky's express disclosure of a programmable logic device (PLD). Pet. 24 (citing Ex. 1003, 5:21–23, Fig. 13). Petitioner cites Dr. Franzon's testimony that one of ordinary skill in the art "would have known that a FPGA is an exemplary PLD" and provides evidence to support its contention. Pet. 24 (quoting Ex. 1002 ¶ 293). Petitioner relies on declaration testimony of Dr. Franzon that, as Petitioner notes, identifies citations to specific passages of prior art references to support his testimony. Pet. 24 (citing Ex. 1002 ¶ 293; quoting Ex. 1035, 1:29–30 ("a field programmable gate array (FPGA) 100, which is one type of PLD"); Ex. 1036, 4:1–9 ("Thus, in a programmable logic device, such as a field programmable gate array (FPGA). . ."); Ex. 1037, 1:13–22; Ex. 1038, Abstract)).

Additionally, Petitioner cites "Zavracky's description of a PLD for a 'user-defined' communication protocol, Ex. 1003, 12:33–36" and Dr. Franzon's testimony that this description would have "suggested to [one of ordinary skill in the art] that a FPGA was [a] type of PLD since the 'user' would be 'defining' that protocol later in the field." Pet. 25 (quoting Ex. 1002 ¶ 294 (citing Ex. 1040; Ex. 1051). Petitioner also relies on Dr. Franzon's testimony that one of ordinary skill in the art "would have been motivated to use a FPGA because a field programmable array was recognized as the correct programmable logic device for such a 'user- defined' network device." Pet. 25 (citing Ex. 1002 ¶ 294). Dr. Franzon's testimony is supported by summary of two papers that describe FPGAs used in that context. *See* Ex. 1002 ¶ 294 (describing Ex. 1040 (using a FPGA-

based firewall); Ex. 1051 (describing using an FPGA to create an "adaptable digital network processor)).

Petitioner also contends that "the combination of Zavracky and Chiricescu teaches or suggests 'a first integrated circuit functional element including a field programmable gate array.'" Pet. 25 (citing Ex. 1002 ¶ 296; Ex. 1004, 232). "Chiricescu literally describes Zavracky as teaching technology 'to build 3-D layered **FPGAs** which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip." Pet. 25 (citing Ex. 1004, 232) (emphasis in Petition); *see* Ex. 1004, 235 n.3 (citing Ex. 1003). Petitioner contends that "the Zavracky-Chiricescu combination yields a modified version of Zavracky's 3D chip stack where Zavracky's 'PLD' layer is implemented as Chiricescu's" FPGA layer. Pet. 25–26 (citing Pet. VII.A.2 (summary of Chiricescu); *see also* Pet. 16 (describing Chiricescu having an FPGA layer").

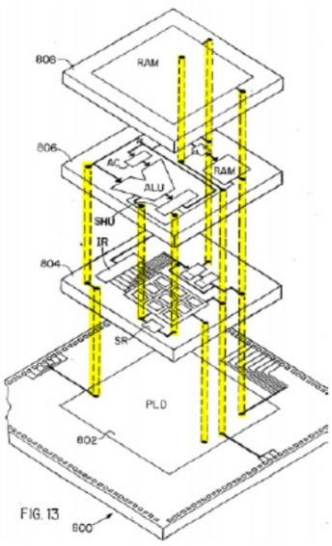
Regarding "at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element" (limitation [1.2]), Petitioner again relies on Zavracky's Figures 12 and 13 as disclosing stacked integrated circuit functional elements. Pet. 26. Petitioner indicates that Zavracky describes Figure 12 as having a "random access memory array." Pet. 26 (citing Ex. 1003, Fig. 12, 12:15–28); Ex. 1003, 12:14–15 ("FIG. 12 presents a stacked microprocessor and random access memory array . . .").

Petitioner quotes Zavracky's teaching of vertically stacked and interconnected circuit element layers that are electrically coupled:

> One significant aspect in the formation of three-dimensional circuits involves interconnecting the layered devices. . . . Via holes are formed through the upper contact areas to gain access to the lower contact areas. . . . Electrical contact between the upper and lower devices is made by filling the via holes 1022 with an electrically conductive material . . . [.]

Pet. 27 (quoting Ex. 1003, 14:51–63; citing Ex. 1003, 2:18–22, 2:27–35, 10:8–21, 10:61–65, Fig. 6).

Petitioner also contends that Zavracky's PLD (on which Petitioner relies as teaching or suggesting the FPGA of the first integrated circuit functional element) is vertically stacked with and electrically coupled to Zavracky's memory array, such as shown in Figures 12 and 13. Pet. 27–28 (Ex. 1003, Fig. 12 (annotated), Fig. 13 (annotated)). Petitioner's annotated version of Zavracky's Figure 13 depicts stacked functional elements and the coupled contact points relied upon by Petitioner:



Pet. 27–28. Zavracky's Figure 13 above as annotated by Petitioner depicts (highlighted) inter-layer via connections in programmable logic array 802, which "can be programmed to provide for user-defined communication protocol between the microprocessor and any off-chip resources." Ex. 1003, 12:29–37.

Regarding limitation [1.3]—"wherein said field programmable gate array is programmable as a processing element," Petitioner relies on Zavracky's disclosure that its "programmable logic array 802" "can be programmed to provide for user-defined communication protocol" and its analysis regarding limitation [1.1] that Zavracky's PLD would teach or suggest the recited FPGA. Pet. 28. For support, Petitioner relies on declaration testimony of Dr. Franzon that one of ordinary skill in the art would have understood Zavracky's programmable logic array to be operating as a processing element. Pet. 28 (summarizing Ex. 1002 ¶ 302). Petitioner, in its

citation, notes that Dr. Franzon's declaration testimony relies on evidence to support its conclusion. Pet. 28 ("Ex. 1002 ¶ 302 (citing Ex. 1040)"). Petitioner also asserts that Chiricescu discloses a FPGA that can be quickly reconfigured to implement arbitrary logic. Pet. 29 (citing Ex. 1004, 233–234).

In its combination of Zavracky, Chiricescu, and Akasaka, Petitioner identifies with particularity "Chiricescu's FPGA and memory" with respect to claim 1's acceleration limitation [1.4]—"wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element." Pet. 29–30. According to Petitioner, Chiricescu's solution to the problem of high configuration time of a FPGA is a memory layer storing configuration information to avoid going "off-chip" to load FPGA reconfiguration data. Pet. 29–30 (citing Ex. 1004, 232, 234; Ex. 1002 ¶¶ 304–07). Petitioner asserts Chiricescu teaches that the FPGA-reconfiguration is accelerated by the data already having been loaded into the memory array. Pet. 30 (Ex. 1004, 234; Ex. 1002 ¶¶ 304–07).

To support its contention, Petitioner relies on passages from Chiricescu and four paragraphs of Dr. Franzon's declaration testimony, which provides reasoning with citations to Chiricescu and to a 1999 reference that predates the earliest filing date claimed by the '214 patent (Ex. 1057).[19] In his declaration testimony cited by Petitioner, Dr. Franzon further explains his conclusion that "Chiricescu's 'cache'

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[19] In Ex. 1002 ¶ 304 Dr. Franzon quotes Pierre Marchal, *Field-Programmable Gate Arrays*, ACM, Communications of the ACM, Vol. 42, No. 4 (April 1999) (Ex. 1057).

memory . . . is functional to accelerate reconfiguration of said FPGA as a processing element," as required by claim 1's acceleration limitation. Ex. 1002 ¶ 307; Pet. 29 (citing Ex. 1002 ¶¶ 304–09); Pet. 30 (citing same). On this basis, Dr. Franzon expressly concludes that Chiricescu's memory is functional to accelerate as recited in claim 1.

Independent claim 2 includes the same limitations as recited in independent claim 1. *Compare* Ex. 1001, 7:56–65*, with id.* at 8:1–15. For those limitations, Petitioner relies on its arguments made with respect to independent claim 1. Pet. 30–31 (Petitioner's contentions regarding claim 2 referencing analysis regarding same limitations in claim 1).

Independent claim 2 additionally recites "said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements." Ex. 1001, 8:7–10. For this limitation, Petitioner relies on its combination of Zavracky, Chiricescu, and Akasaka. Pet. 31. In its combination for this limitation, Petitioner identifies Akasaka's description of electrical coupling of active layers through via holes and asserts Akasaka's 3D IC (shown in Akasaka's Figure 4) is similar to Figure 4 and corresponding the description in the '214 patent. Pet. 31–32 (citing Ex. 1001, 4:63–5:1, 5:7–11, 5:16–26, Fig. 4; Ex. 1005, 1705, 1707; Ex. 1002 ¶¶ 327–32).

The record supports Petitioner's position. We find Akasaka's active circuit layers connected electrically through via holes teach or suggest the recited "integrated circuit functional elements that are coupled by a number of contact points distributed

throughout the surfaces of said functional elements." Akasaka's active layers in its 3D-IC are integrated circuit functional elements. (Ex. 1005, 1705 ("Each layer or set of several active layers can have its own function")).

Akasaka describes "exchang[ing] signals between upper and lower circuit layers through via holes in 3-D ICs" and further specifics that "[e]ach active layer is connected electrically via holes, and signals can be transferred between the layers." Ex. 1005, 1705, 1707; Fig. 4 (showing via-hole connections between two active layers in a 3-D integrated circuit). Akasaka indicates "[s]everal thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or vice versa) through them." Ex. 1005, 1705. That Akasaka uses the term "holes" rather than the recited "contact points." The '214 patent, however, describes "contact points" shown in its Figure 4 also as via holes. Ex. 1001, 4:63–5:1 (describing Fig. 4 as depicting a stack of dies including "microprocessor die 64, memory die 66, and FPGA die 68, all of which have a number of corresponding contact points, or holes 70"); *see* Ex. 1002 ¶ 327 (Dr. Franzon testifying that the '214 patent "describes 'contact points' as 'holes' or through-silicon contacts" (quoting Ex. 1001, 4:63–5:1, 5:7–8, 5:16–17 for support)).[20]

Regarding the requirement that the contact points be "distributed throughout the surfaces of said

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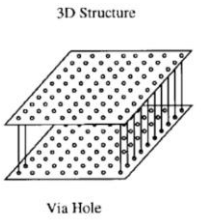
[20] Dr. Franzon testimony cites to the '035 patent specification and notes that equivalent disclosures exist in the other challenged patents. Ex. 1002 ¶ 327. The '214 patent includes the portions cited by Dr. Franzon at the citations noted above.

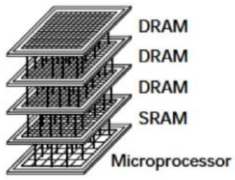
functional element," we agree with Petitioner that the combination of Zavracky and Akasaka would have taught or suggested this feature. *See* Pet. 32–33 (citing Ex. 1003, 6:43–47, 13:43–47, 14:52–63; Ex. 1005, 1705; Ex. 1002 ¶ 332). More specifically, this feature is at least suggested by Zavracky's teaching of 3D stack elements where "openings or via holes" providing inter-layer connections "can be placed anywhere" and "are not limited to placement on the outer periphery" and Akasaka's teaching of "tens of thousands of via holes." Ex. 1003, 6:43–47, 13:43–47, 14:52–63; Ex. 1005, 1705; *see* Pet. 32 (citing Ex. 1003, 6:43–47, 13:43–47, 14:52–63; Ex. 1005, 1705); *see also* Ex. 1005, Fig. 4 (showing three sets of via holes in active layers, including the center set of via holes placed away from two of the edges of the active layers); Ex. 1002 ¶ 331 (Dr. Franzon describing Akasaka as "teaching that 'tens of thousands of via holes' can be distributed throughout the surface of the stacked elements (as shown in Akasaka's Figure 4)").

We credit Dr. Franzon's testimony in this regard because it is consistent with the descriptions in Zavracky and Akasaka as noted above. Furthermore, Dr. Franzon provides additional citations to prior art references to support his opinion that structures of "stacked [integrated circuit] elements with contact points (e.g., via holes) distributed across the surfaces of elements" were "ubiquitous in the prior art" and that one of ordinary skill in the art "would have been well acquainted with such structures." Ex. 1002 ¶ 332 (citing Ex. 1020, 9–10 ("'through hole vias' provide 'array of contacts [that] are used to provide vertical interconnections'"), Fig. 4; Ex. 1021, Figs. 4, 17 ("more than 10^5 interconnections per chip"); Ex. 1028, Fig. 9,

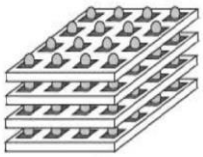
1 ("'10,000' vias with enlarged diagram to show structure")). For example, Dr. Franzon included three figures reprinted below:



Franzon,
Ex. 1020 Fig. 4



Koyanagi,
Ex. 1021 Fig. 1(a)



Alexander,
Ex. 1028, Fig. 2(b)

Each of the three figures show stacked layers with via holes distributed across the element layers. *See* Ex. 1020, Fig. 4; Ex. 1021, Fig. 1(a); Ex. 1028, Fig. 2(b).

For these reasons, we find that Petitioner's combination of Zavracky, Chiricescu, and Akasaka teaches or suggests "said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements," as recited in claim 2.

Independent claims 26 and 27 each recite many of the limitations also recited in independent claims 1 and 2. For example, like claim 2, independent claim 27 recites "said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements."

Independent claims 26 and 27, however, "wherein said memory array is functional to accelerate *external memory references to said processing element*," rather than reciting "functional

to accelerate reconfiguration *of said field programmable gate array as a processing element*."

Petitioner relies on its arguments made with respect to independent claims 1 and 2 for the claim limitations recited in independent claims 26 and Pet. 36–37 (Petitioner's contentions regarding claims 26 and 27 referencing analysis regarding limitations in claims 1 or 2).

b. Disputed Limitations in Independent Claims 1, 2, 26 and 27

A central issue in this proceeding is whether Petitioner's combination of Zavracky, Chiricescu, and Akasaka teaches or suggests "the functional to accelerate" limitations recited in the independent claims.

(i) Petitioner's Contentions

For these limitations, in its combination of Zavracky, Chiricescu, and Akasaka, Petitioner identifies with particularity "Chiricescu's FPGA and memory" used to address the problem of "the high configuration time of an FPGA." Pet. 29–30. To address this problem caused by having to load configuration data from off-chip memory, Chiricescu uses a "memory layer" in which "random access memory is provided to store configuration information" to avoid going "off-chip" to load FPGA reconfiguration data. Pet. 29–30 (citing Ex. 1004, 232, 234; Ex.1002 ¶¶ 304–07). In addition to the numerous short vias of the combination providing acceleration, Petitioner also asserts Chiricescu teaches that the FPGA-reconfiguration is accelerated by the data already having been loaded into the memory array. Pet. 30 (citing Ex. 1004, 234; Ex. 1002 ¶¶ 304–07).

To support its contention, Petitioner relies on passages from Chiricescu and four paragraphs of Dr. Franzon's declaration testimony, which provides reasoning with citations to Chiricescu and to a 1999 reference that predates the earliest filing date claimed by the '214 patent (Ex. 1057). In his declaration testimony cited by Petitioner, Dr. Franzon further explains his conclusion that "Chiricescu's 'cache' memory . . . is functional to accelerate reconfiguration of said FPGA as a processing element," as required by claim 1's "functional to accelerate" limitation. Ex. 1002 ¶ 307; Pet. 29 (citing Ex. 1002 ¶¶ 304–09); Pet. 30 (citing same). Thus, Dr. Franzon expressly concludes that Chiricescu's memory is functional to accelerate as required in claim 1.

As noted previously, Petitioner's combination "fold[s] in Chiricescu's teachings (including using stacked memory to reconfigure a FPGA) with Zavracky's 3D stacks" to lead to significant improvement in reconfiguration time, among other reasons. Pet. 18–19. Thus, as noted above, Chiricescu's stacked memory to reconfigure a FPGA accelerates FPGA reconfiguration because the needed data is already stored in Chiricescu's stacked memory.

Petitioner relies on this analysis for the same limitation in independent claim 2 and for "said memory array is functional to accelerate external memory references to said processing element," as recited in independent claims 26 and 27. Petitioner adds in the context of claims 26 and 27 that the relevant analysis is "discussing acceleration of FPGA reconfiguration through acceleration of external memory references." Pet. 37 (claim 26), 38 (claim 27).

(ii) *Patent Owner's Contentions*

Patent Owner contends that Zavracky, Chiricescu, and Akasaka alone or as combined by Petitioner fail to teach or suggest "wherein said memory array is functional to accelerate *external memory references to said processing element*" recited in claims 26 and 27 and fail to teach or suggest "wherein said memory array is functional to accelerate *reconfiguration of said field programmable gate array as a processing element*," as recited in claims 1 and 2. PO Resp. 18–22 (claims 26 and 27), 22–23 (claims 1 and 2).

Patent Owner first presents contentions regarding claims 26 and 27 (which Patent Owner argues together). *See PO Resp.* 18–22; PO Sur-reply 2–10. Patent Owner then addresses claims 1 and 2 (which Patent Owner groups together), like Petitioner does, by indicating the arguments addressing claims 26 and 27 also show claims 1 and 2 to be patentable. PO Resp. 22–23; PO Sur-reply 10.

According to Patent Owner, Petitioner's combination fails because the claims require "structure ***provided within the memory array*** *(i.e.* the wide configuration data port disclosed in the '214 Patent) that is responsible for accelerating the programmable array's accelerated external memory references. PO Resp. 18–19 (citing Ex. 2011 ¶¶ 53–54); PO Sur-reply 3 (indicating Petitioner's proposed combination does not "include a wide configuration data port as the claimed invention requires"). For the reasons explained previously (Section II.C), we do not agree with Patent Owner.

Patent Owner correctly notes that the '214 patent "provides accelerated memory references due to its technique of stacking a programmable array with a memory die using through-silicon vias (TSVs)." PO Resp. 18–19 (quoting Ex. 1001, 5:16–26). Patent Owner then contends "Chiricescu's 'RLB BUS' that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the '214 Patent" and "loads the configuration data 'in a byte serial fashion and must configure the cells sequentially.'" PO Resp. 19–20 (citing Ex. 2012, 80:12–17; Ex. 1001, 4:51–58; Ex. 2011 ¶ 55). For these reasons, Patent Owner asserts, that "Chiricescu fails to disclose any technique for accelerating external memory references over the baseline of a narrow configuration data port that loads data 'in a byte serial fashion.'" PO Resp. 20.

Contrary to Patent Owner's arguments, Petitioner persuasively argues and as summarized above, the Petition relies on the combined teachings of Zavracky, Chiricescu, and Akasaka to teach the "functional to accelerate clause." *See* Pet. Reply 4–7; Pet. 29–30. Patent Owner's arguments unduly focus on Chiricescu alone without sufficiently considering Petitioner's combination of Zavracky, Chiricescu, and Akasaka. *See* Pet. Reply 10–11 (citing Pet. 14–30; Ex. 2012, 29:15–32:15).

Petitioner also persuasively shows that Patent Owner "misrepresents Dr. Franzon's testimony" regarding an alleged narrow port in Chiricescu. *See* Pet. Reply 11 (addressing PO Resp. 19–20). As Petitioner persuasively argues,

> Dr. Franzon's cited testimony: (1) has nothing to do with Chiricescu; (2) was given in response to a

> question about Trimberger; and (3) was discussing the connection to "an off- chip memory" (80:11). Ex. 2012, 80:10–22.

Pet. Reply 11.

Dr. Franzon's cited deposition testimony supports Petitioner. Specifically, Dr. Franzon's cited deposition testimony refers to Trimberger in the context of "off-chip memory that loads in through the data port," and Dr. Franzon testifies that one of ordinary skill in the art "would interpret figure 5 as [including an undepicted] similar narrow structure on the left of the very wide configuration data port" to load data from an external source." *See* Ex. 2012, 80:3–22. In other words, Dr. Franzon's testimony does not describe Chiricescu's stacked memory layer as using a narrow port to transfer reconfiguration data to the RLB (with FPGA gates) layer from this "on-chip" memory within the 3D stack, as Patent Owner alleges. *See* Ex. 1004, Fig. 2.

As Petitioner also argues, Patent Owner's "'narrow data port' arguments are contrary to Chiricescu's teachings" and do not address the combined teachings of Chiricescu, Zavracky, and Akasaka. Pet. Reply 11 (citing PO Resp. 19–20). Petitioner notes that Zavracky describes "interconnects as being 'placed anywhere on the chip' without restriction." Pet. Reply 11 (emphasis added) (quoting Ex. 1004, 232). In addition, Petitioner notes that Chiricescu "discloses 'three separate layers with metal interconnects [including a "memory layer"] between them.'" Pet. Reply 11 (quoting Ex. 1004, 232) (bracketed text added by Petitioner) (emphasis omitted).

In other words, by placing vias anywhere throughout the different dies as Chiricescu and the combined teachings suggest, the combined teachings distinguish over a narrow data port, where Petitioner provides well-known reasons for employing wide data ports, such as allowing for increased bandwidth and parallelism. *See* Pet. 18–20; Ex. 1001, 5:16–21 (describing "through-die array contacts 70 . . . routed up and down the stack in three dimensions" as "not known to be possible with any other currently available stacking techniques since they all require the stacking contacts to be located on the periphery of the die," so that by placing contacts throughout, "cells that may be accessed within a specified time period is increased") (emphasis added).

As Petitioner also persuasively argues, even if the claims require a wide configuration data port, according to Patent Owner's expert in the IPR2020-01020, IPR2020-01021, and IPR2020-01022, a "configuration data port . . . is . . . just a data port used for configuration . . . And data port is just an interface to send data from one place to another." Reply 9 (quoting Ex.1075, 163:8–163:21). "And 'the reason it's a very wide configuration data port is because it has a lot of connections through these TSVs between the memory die and the FPGA die.'" Pet. Reply 9 (quoting Ex. 1075, 157:23–158:3 (Dr. Chakrabarty agreeing with this statement).

In other words, under Petitioner's persuasive showing, even if the challenged claims require a wide configuration data port, the combined teachings meet the claims for the reasons noted. Pet. Reply 9 ("The Zavracky, Chiricescu, and Akasaka Combination provides the 'memory . . . accelerate' limitations even

under [Patent Owner's] flawed construction" that the wide configuration data port is responsible for accelerating.). Petitioner persuasively shows that the Zavracky-Chiricescu-Akasaka 3D module uses numerous vias throughout the dies to transfer data between the dies—i.e., acting as a wide configuration data port functional to accelerate all manner of data and signals in parallel. *See, e.g.*, Pet. 17 (showing that Akasaka teaches that "'tens of thousands of via holes' permit parallel processing" by utilizing the many interconnections; as a result of this parallel processing, "the signal processing speed of the system will be greatly improved"; and due to "shorter interconnection delay time and parallel processing" made possible from the area-wide interconnects, the processing of data between layers is accelerated such that "twice the operating speed is possible in the best case of 3-D ICs" (quoting Ex. 1005, 1705)), 20 (arguing that "it was a predictable advantage and also suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity" (citing Ex. 1002 ¶ 233 (quoting Ex. 1005, 1705)). Petitioner also shows that "[i]t was well known that 'interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems,' and that 'wide buses are very desirable' and were made possible by 3-D stacking." Pet. 12.

Therefore, Petitioner shows that the numerous via connections between the memory die and FPGA connect to the memory array to render the "memory array functional to accelerate memory references to

the processing element," as claim 1 requires. *See, e.g.*, Pet. 20–21 (showing that Akasaka's numerous connections would have motivated a POSITA to replicate common data memory, and "increase bandwidth and processing speed through better parallelism and increased connectivity").

Additionally, Patent Owner argues that, because Dr. Franzon did not provide a baseline against which to measure acceleration, Petitioner has not demonstrated "the combination of references 'accelerates external memory references to said processing element' over the baseline of the relatively narrow configuration port distinguished in the '214 Patent (and taught in Chiricescu)." PO Resp. 20–21 (citing Ex. 2012, 25:21–26:23; Ex. 1001, 1:50–55, 4:27–32; Ex. 2011 ¶ 56). Petitioner also persuasively addresses Patent Owner's argument that the claims require acceleration over a "baseline." *See* PO Resp. 20–21; Reply 11–12. Petitioner points to Dr. Franzon's testimony "that the Zavracky-Chiricescu-Akasaka combination provides acceleration compared to the baseline of other prior art with different structural characteristics." Pet. Reply 11–12 (citing Ex. 1002 ¶¶ 212, 215–17, 304–05; Ex. 2012, 29:15–33:15, 28:9–21).

Petitioner also persuasively addresses Patent Owner's argument that "external memory references . . . are not data, but are instructions directed to a particular place memory [sic] address in memory." PO Resp. 12 (including [sic] annotation). Petitioner quotes Dr. Franzon's declaration testimony:

> Chiricescu is teaching to use that memory as a "cache"… By doing so, the FPGA's external memory references… will be accelerated because

> [they] will "hit" in the "cache" and be returned from the on-chip memory without having to go off- chip. Chiricescu is thus teaching to the POSITA to accelerate memory lookups….

Pet. Reply 12 (block quoting Ex. 1002 ¶¶ 215–16; citing Ex. 2012, 42:9–14, 48:6–50:1).

In response to Petitioner's Reply, Patent Owner contends that Dr. Franzon testified that external memory references could be located on an off-chip memory die stacked with the programmable array die and, therefore, Dr. Franzon testified that it is the "off-chip memory on the second integrated die element [that] is functional to 'accelerate external memory references to the processing element.'" PO Sur-reply 7 (block quoting Ex. 2012, 42:21–43:3). Patent Owner concludes that Petitioner's combination of Zavracky, Chiricescu, and Akasaka "does not teach or suggest the claimed structure under any construction" because Petitioner's combination of Zavracky, Chiricescu, and Akasaka "does not satisfy a 'memory array [is] functional to accelerate external memory references to said processing element'" and does not "include a wide configuration data port as the claimed invention requires." PO Sur-reply 3. Patent Owner, however, misinterprets Dr. Franzon's testimony that concerned the plain and ordinary meaning of "external memory references" as indicating what element (i.e., off-chip memory) would be performing an external memory reference. *See* Ex. 2012, 4215–44:45.[21] For this reason, we do not agree with Patent

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[21] Ex. 2012, 42:15–43:3 (discussing meaning of "external memory reference" before a break), 43:13:44:3 (characterizing topic before the break as "discussing the plain and ordinary memory of the

Owner's characterization of Dr. Franzon's deposition testimony.

Patent Owner also argues, in response to Petitioner's Reply, that "[t]he entire point of Chiricescu is that it achieves accelerated FPGA configuration by storing configuration data 'on-chip' so that it does not need to load configuration data from off-chip." Sur-reply 4-5. Patent Owner also argues that "all off-chip connections are carried out through a typical narrow configuration data port, that suffers the same problems as the prior art distinguished in the '214 Patent." PO Sur-reply 5. Patent Owner then argues that "moving Chiricescu's cache memory off-chip (i.e., into Zavracky's 3D stacked memory die) eliminates the benefit gained from moving the memory on-chip, [so] a POSITA would not have contradicted Chiricescu's fundamental teachings to arrive at Petitioner's proposed combination." PO Sur-reply 5.

We do not agree with Patent Owner's position. Patent Owner does not sufficiently address Chiricescu's memory and FPGA layers that are short "interlayer vias" "placed anywhere on the chip" within the same 3D stack and, thus, is not off-chip. As Petitioner notes, Dr. Franzon described "routine use of on-chip area-wide connections in 3D stacks, including his prior work." Reply 17–18 (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶ 65; Ex. 1020; *see also* Ex. 1004, Fig. 2, 232 § 1 (describing "on chip random access memory . . . provided to store configuration memory"—i.e., the memory layer of Figure 2).

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term 'external memory references'"), 44:4–4 (questioning "what element would be performing this type of memory reference").

Patent Owner contends that "the movement of *Chiricescu's* on-chip cache memory to *Zavracky's* off-chip memory would throttle" speed gains. Sur-reply 5. We do not agree with Patent Owner. In the context of Chiricescu's teachings and Petitioner's showing, Zavracky includes memory in a stack of chips connected by numerous short vias as Petitioner shows and as discussed above. *See, e.g.*, Pet. 14–16, 23–28. Patent Owner's attempt to conflate Zavracky's modified stack of chips as "off-chip" such that "all off-chip connections are carried out through a typical narrow configuration data port" is not supported. *See* Sur-reply 5. Chiricsescu describes loading configuration data from "memory off-chip" as "significantly" and distinctly slower (Ex. 1004, 234) than loading it from an "on-chip random access memory layer" (*see* Ex. 1004, 232) within the stacked layers of the disclosed 3D FPGA. *See* Ex. 1004, 234, 232, Fig. 2. As Petitioner persuasively shows throughout its briefing, Zavracky's stack of chips connected by numerous vias, as modified by Akasaka's and Chiricescu's teachings, operates just like Chiricescu's "on-chip" circuit layers in a single chip connected by numerous vias in terms of speed and acceleration. *See* Pet. Reply 6 ("Zavracky's short interior 'inter-layer connectors' to stacked 'random access memory . . . results in reduced memory access time, increasing the speed of the entire system,'" and "Chiricescu also teaches the acceleration advantages and 'significantly improve[d FPGA] reconfiguration time' achieved by its interconnected layers, including a memory layer configured as a cache for fast access to 'configuration data… from memory off-chip.'" (quoting Ex. 1003, 11:63–12:2; Ex. 1004, 232)), 7 (noting Akasaka's "acceleration advantages" based on

"teaching, e.g., that '[h]igh- speed performance is associated with shorter interconnection delay time and parallel processing' and that 'shortening of interconnections and signal transfer through vertical via holes in the 3-D configuration provides advantages for the design of large-scale systems.'" (quoting Ex. 1005, 1705)). In other words, as Petitioner shows, in addition to "stacking techniques," "[t]he Zavracky-Chiricescu-Akasaka Combination also discloses the other ways that the '214 patent even arguably implies increases speed—i.e., through caching, the use of short electrical paths, or significantly increased number of connections." Pet. Reply 8 (citing Pet. 14–30).

Patent Owner agrees that "Chricescu says . . . [that] "[t]he elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application." Sur-reply 4 (quoting Ex. 1004, 234). Patent Owner argues, however, that "Petitioner concocts its hypothetical structure based on its demonstrably false claim that Chiricescu's improved FPGA reconfiguration time is 'achieved by its interconnected layers, including a memory layer configured as a cache for fast access to "configuration data . . . from memory off-chip."' Sur-reply 4 (quoting Reply 6 (quoting Ex. 1004, 234)). Patent Owner contends that "Chiricescu says just the opposite." PO Sur-reply 4 (citing Ex. 1004, 234).

Contrary to Patent Owner's argument, Petitioner argues that Chiricescu improves FPGA reconfiguration time because Chiricescu's cache pre-stores and holds configuration data on-chip that it obtains from an external source (i.e., off-chip

memory)—so that the FPGA need *not* access that external (off-chip memory) source to load the FPGA through a typical narrow configuration data port during FPGA reconfiguration. *See* Pet. Reply 6 (describing acceleration "achieved by its interconnected layers, including a memory layer configured as a cache for fast access to 'configuration data . . . from memory off-chip'" (quoting Ex. 1004, 232); Ex. 1004, 234 ("The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application.").

Patent Owner additionally contends that Petitioner's combination would improperly alter Chiricescu's principle of operation. PO Resp. 27–28 (arguing Petitioner's combination "would improperly alter Chiricescu's principle of operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB bus and its 'routing layer'"). As Petitioner notes, Patent Owner's argument is based on a misunderstanding of Petitioner's combination that does not modify Chiricescu but rather "folds in Chiricescu teaching with Zavracky's 3D stacks." Pet. Reply 15 (addressing Patent Owner's principle of operation argument); *see* Pet. 18–19 ("The POSITA would have been encouraged to fold in Chiricescu's teachings (including stacked memory to reconfigure the FPGA) with Zavracky's 3D stacks, understanding it would lead to 'significant[] improvement in the reconfiguration time.'"). In response to Petitioner's Reply, Patent Owner indicates Chiricescu addresses "the problem of 'loading configuration data on an as needed basis from memory off-chip' was to move that memory on-chip." PO Sur-reply 5.

We do not agree with Patent Owner that Petitioner's combination alters Chiricescu's principle of operation because, as discussed throughout this decision, Petitioner's combination relies on Zavracky's stack of chips connected by numerous vias (as modified by Akasaka's and Chricescu's teachings) that operate in terms of speed and acceleration like Chiricescu's "on-chip" circuit layers in a single chip connected by numerous vias. *See, e.g.,* Pet. 18–22; Pet. Reply 5–6.

Patent Owner further contends that Dr. Franzon "concedes that Akasaka's thousands of connections would not and could not be used in Petitioner's hypothetical structure such that the 'memory array [is] functional to accelerate external memory references to said processing element." PO Sur-reply 5–6 (citing Ex. 2012, 80:10–17).

We do not agree with Patent Owner's characterization of Dr. Franzon's testimony. First, the cited portion of Dr. Franzon's testimony did not address "Akasaka's thousands of connections" as Patent Owner contends. Rather, Dr. Franzon's testimony was made in the context of the implicit similarity of the structure of another reference and in the context of loading data from an external source—Trimberger (Ex. 1006)—and undepicted narrow port implicit "on the left of" Figure 5 of the challenged patent.[22] Ex. 2012, 80:3–6 (Dr. Franzon testifying, "So if there's 100,000 memory circuits in Trimberger, it can't reload all those memory contents within one

[22] Dr. Franzon's testimony concerned his declaration testimony (Ex. 1002) concerning four patents, one of which was the '214 patent. Ex. 2012, 4:14– 5:13, 8:4–8. The '214 patent also includes Figure 5 of the '226 patent.

clock cycle [from an external source]. The same would be true of '226 [patent]. The structure in figure 5 of '226 [patent] does not show anything on the left of the very wide configuration data port."); 80:15–22 (Dr. Franzon testifying, "you wouldn't have thousands of bits wide access [from an external source] to the DRAM in a normal memory structure in this time frame. So there would be a similar narrow structure—[one of ordinary skill in the art] would interpret figure 5 as a similar (undepicted) narrow structure *on the left of the very wide configuration data port*" (emphasis added)).

Second, Patent Owner's arguments do not undermine Petitioner's combination of Zavracky, Chiricescu, and Akasaka having multiple vertical vias in the stacked memory chip structure of Zavracky, as modified by the teachings of Chiricescu and Akasaka, to accommodate the memory array operating as a cache memory to accelerate the loading of the reconfiguration data. *See* Pet. 18–22, 28–32. Petitioner notes, for example, that Akasaka suggests "that applying Akasaka's distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity.'" Pet. 18 (citing 1002 ¶ 233 (quoting Ex. 1005, 1705)).

Patent Owner also responds to Petitioner's Reply by asserting that "Dr. Franzon admits that it is the structure of the wide configuration data port, including buffer cells, that allows for the acceleration of external memory references to the programmable array." PO Sur-reply 6 (citing Ex. 2012, 77:5–15, 42:21–43:3). Patent Owner characterizes that testimony as indicating "it is a new and improved

configuration (not discussed in any of Petitioner's myriad of references) that allows for the memory array to be functional to accelerate external memory references to the processing element of the programmable array." PO Sur-reply 6–7.

Here, too, we do not agree with Patent Owner's characterization of Dr. Franzon's cited testimony. First, Dr. Franzon does not characterize the structure of the wide configuration data port as including buffer cells. Rather, Dr. Franzon indicates the "exemplary wide configuration data port 82 depicted in figure 5 [of the challenged patent] shows a direct path to every buffer cell." Ex. 2012, 77:7–10. As discussed previously, Figure 5 depicts the wide configuration data port as a "black box" and that depiction does not include the buffer cells as part of the "black box" wide configuration data port 82. *See* Section II.C (Claim Construction) above. Second, Dr. Franzon's testimony at page 77 describes how the wide configuration data port shown in Figure 5 of the challenged patent is able to "store a configuration in the buffer cell and upload it to the logic cell in one clock cycle" and that the same structure is shown in Trimberger. Ex. 2012, 77:5–15. Rather than describing the wide configuration data port of Figure 5 of the challenged patent as "a new and improved configuration (not discussed in any of Petitioner's myriad of references" (as Patent Owner alleges), Dr. Franzon states that it is the "same structure" as shown in a prior art reference (Trimberger, Ex. 1006). Third, Dr. Franzon's cited testimony on pages 42–43 opines that the recited external memory reference is located in off-chip memory. Patent Owner does not sufficiently explain how the *location* of external memory references

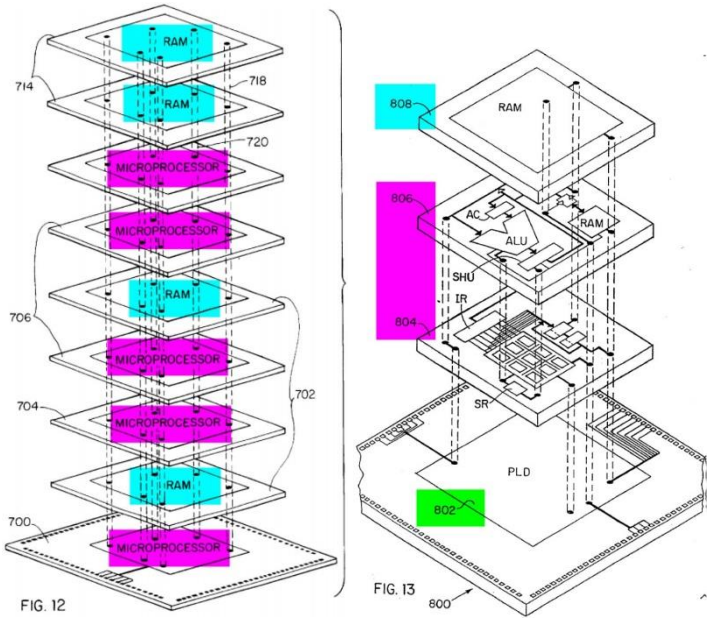
relates to allowing for the memory array to be functional to accelerate those references.

4. *Dependent Claims 4, 6, 29, and 31*

Petitioner presents evidence that dependent claims 4, 6, 29, and 31 would have been obvious over Zavracky, Chiricescu, and Akasaka. Pet. 34– 36, 38. Patent Owner does not present separate arguments for limitations additionally cited by these dependent claims.

Claim 4 depends from independent claim 2 and additionally recites "further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements" for which Petitioner partly relies on Zavracky's Figures 12 and 13. Pet. 34–35. Claim 29, depends from independent claim 27, and additionally recites the same limitation as recited in claim 4. Petitioner's argument regarding dependent claim 29 partly relies on Petitioner's argument for claim 4. Pet. 38.

For the recited third integrated circuit functional element, Petitioner identifies the microprocessors shown in Zavracky's Figures 12 (microprocessors on their own) and 13 (a multi-layer microprocessor). Pet. 34. Petitioner's annotated Figures 12 and 13 are depicted below:



Zavracky's Figure 12 "presents a stacked microprocessor and memory array." Ex. 1003, 12:14–15, Fig. 12. Zavracky describes first microprocessor layer 700 that "shares random access memory 702 on the second layer, [with] another microprocessor 704 located above the random access memory." Ex. 1003, 12:17–20. Zavracky describes "address 720, and data 718 buses [that] run vertically through the stack by the use of inter- layer connectors." Ex. 1003, 12:25–27. Zavracky's Figure 13 depicts "programmable logic array 802 . . . fabricated upon the first layer 800. The second 804 and third 806 layers comprise a multi-layer microprocessor, with random access memory on the fourth layer 808." Ex. 1003, 12: 31–34. Notably, Zavracky indicates programmable logic array 802 "can be formed in any of the layers of a multilayer

structure as described elsewhere herein." ex. 1003, 12:37–39.

Claim 6 depends directly from claim 4 and indirectly from independent claim 2. Claim 6 additionally recites "said third integrated circuit functional element includes an I/O controller" for which Petitioner partly relies on Zavracky's controller depicted in Figure 13. Pet. 35–36. Claim 31, depends from independent claim 29, and additionally recites the same limitation as recited in claim 4. Petitioner's argument regarding dependent claim 31 partly relies on Petitioner's argument for claim 6. Pet. 38.

Petitioner identifies controller depicted on multi-layer microprocessor 804 in Figure 13 and also shown and labeled as "CONTROLLER" in Figure 11. Pet. 35. Based on Zavracky's express descriptions of the "controller," Petitioner persuasively argues, with support of Dr. Franzon's testimony, that one of ordinary skill in the art "would have understood Zavracky as describing an I/O controller, which arbitrates the inputs and outputs to a shared communication bus." Pet. 35–36 (quoting Ex. 1003, 5:54–60, 5:49–52, Ex. 1002 ¶¶ 324–25). We find Dr. Franzon's testimony in this regard as credible because he provides persuasive explanation and analysis with comparisons between specific passages of a prior art reference (Ex. 1052) and Zavracky's description. Ex. 1002 ¶¶ 324–25 (citing Ex. 1052, Abstract, 4:65–5:1; Ex. 1003, 5:54–60, 5:49–52 among others).

5. *Summary*

After a full review of the record, including Patent Owner's Response and Sur-reply and evidence, Petitioner shows by a preponderance of evidence that

the combined teachings of Zavracky, Chiricescu, and Akasaka would have rendered obvious claims 1, 2, 4, 6, 26, 27, 29, and 31.

E. *Asserted Obviousness of Claims 3 and 28*

Petitioner contends claims 3 and 28 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Satoh. *See* Pet. 1, 38– 42.

1. *Disclosure of Satoh*

Satoh discloses a semiconductor integrated circuit incorporating a variable logic circuit and specifically a Field Programmable Gate Array (FPGA). Ex. 1008, 46.[23] Satoh also describes testing a semiconductor integrated circuit "incorporating a variable logic circuit (FPGA) for outputting a signal indicating whether or not a circuit is normal and forming a given logic [and] a memory circuit capable of reading and writing data." Ex. 1008, 46. Satoh states that "the variable logic circuit (FPGA) performs a self-test, a memory test circuit is built for testing the memory in accordance with a specified algorithm with only the basic logic cells exclusive of defective parts by using information indicating the defective parts obtained by the self-test, and the memory circuit is tested." Ex. 1008, 46.

Satoh also describes "configuring in the variable logic circuit a memory tester circuit that generates a specified test signal and an expected value signal based on a specified algorithm using only normal basic logic cells, supplies the test signal to the memory circuit, compares the output signal obtained as a

[23] We cite to the page numbers in the header of Sato, as is Petitioner's practice.

result from the memory circuit with the expected value signal." Ex. 1008, 49.

2. *Claims 3 and 28*

Claim 3 depends from independent claim 2, and claim 28 depends from independent claim 27. Claims 3 and 28 each further recite "wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element."

a. Petitioner's Combination

For claims 3 and 28, Petitioner relies on a combination of Zavracky, Chiricescu, Akasaka, and Satoh. Pet. 38–39. Petitioner contends that in the Zavracky-Chiricescu-Akasaka-Satoh combination, "the test signal is sent through the contact points between the FPGA of the first IC die element and the memory of the second IC die element, which is how those elements are stacked and electrically coupled." Pet. 41–42 (citing Ex. 1002 ¶¶ 357–59).

Regarding the requisite reason to combine the references, Petitioner relies on Dr. Franzon's declaration testimony that "[i]t was well-known to test stacked modules in order to avoid the expense and waste of silicon by creating 'dead' chips, and improve yield." Pet. 40 (citing Ex. 1002 ¶ 241; indicating Ex. 1002 ¶ 241 further cites Ex. 1009; Ex. 1043). Petitioner indicates that "Satoh specifically praised the use of an FPGA to test 'memory circuits' for 'improving yield and productivity of the semiconductor integrated circuit.'" Pet. 40 (quoting Ex. 1008, 47:23–27).

Additionally, Petitioner further relies on Dr. Franzon's testimony for other reasons one of ordinary

skill in the art would have combined Satoh's testing functionality with the 3D chip of Zavracky-Chiricescu-Akasaka:

> Recognizing the need to test the 3D stack of the Zavracky- Chiricescu-Akasaka Combination, the POSITA would have sought out Satoh's teaching of using a FPGA for testing the co- stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity. Ex. 1002 ¶242. Moreover, (4) a FPGA is reusable: after being configured for testing in manufacture, the FPGA would then be reconfigured for its normal "in the field" purpose. *Id.* (citing Ex. 1045 ("Another advantage . . . is that after testing is complete, the reconfigurable logic (FPGA 28) can be reconfigured for post-testing adapter card functions."); Ex. 1046).

Pet. 40.

Petitioner also relies on Dr. Franzon's declaration testimony in asserting that one of ordinary skill in the art would have had a reasonable expectation of success:

> It was well known to use a FPGA to test circuitry with 2-D chips as taught by Satoh. Ex. 1002 ¶241 (citing Ex. 1043). The POSITA would have recognized Satoh's teaching would readily apply to the 3-D chip elements in the Zavracky-Chiricescu- Akasaka Combination. This includes because such a combination would have been a routine use of an FPGA, whose testing ability was not dependent on structure. Ex. 1002 ¶¶242–43.

> The result of this combination would have been predictable, by known FPGA testing to the 3D stack according to known methods to yield a predictable result. Ex. 1002 ¶244.

Pet. 41.

b. Patent Owner's Contentions

Patent Owner relies on the same unavailing arguments it advances with respect to the challenged claims addressed above. *See* PO Resp. 39 ("Because Petitioner does not contend that Satoh cures any of the deficiencies of the combination of Zavracky, Chiricescu, and Akasaka, as discussed above with respect to Ground 1, its reliance on the same rationales for Ground 3 also fail.").

Patent Owner also argues that "Petitioner's contention that [one of ordinary skill in the art] would be motivated to make the combination because it was well-known to test stacked die and Satoh tested memory elements on the same semiconductor chip (*see* Petition at 40) is divorced from the claimed invention." PO Resp. 39–40. Patent Owner contends that "Petitioner's generic rationale for using FPGAs for testing is wanting in particularity as to why a POSITA would combine the references as recited in the Challenged Claim." PO Resp. 40. Patent Owner contends that Petitioner's rationale fails "as it lacks sufficient explanation of how or why [one of ordinary skill in the art] would have been motivated to use Satoh's FPGA for testing with the hypothetical 3-D structure of Zavracky- Chiricescu-Akasaka 'in the way the claimed invention does.'" PO Resp. 40. (quoting *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012)).

Patent Owner contends that "[w]hether the use of Satoh's FPGA is beneficial for testing does not sufficiently explain why a POSITA would have combined the references to yield the claimed invention." PO Resp. 40–41.

c. Analysis

Petitioner provides specific reasons related to specific recitations in the claims as outlined above, including tying Satoh's testing of a memory array using FPGA testing circuitry to the similar claim elements in claims 3 and 28. Petitioner's arguments are supported by citations to Satoh and Dr. Franzon's declaration testimony that in this regard provides persuasive explanation consistent with specific descriptions of relevant references cited for support. Pet. 40–41 (citing Ex. 1008, 47:23–27; Ex. 1002 ¶¶ 241–44); *see* Ex. 1002 ¶ 241 (citing Ex. 1020, 12; Ex. 1009, 254; 1043, [36], Ex. 1008, 47:23–27), ¶ 241 (citing Ex. 1045, Ex. 1046), ¶ 243 (citing Ex. 1021, Abstract; Ex. 1003, Abstract, 2:9–13, 3:58–67; Ex.1008, 3); ¶ 244 (citing Ex. 1043).

For example, Petitioner identifies using Satoh's FPGA test circuitry and memory testing teachings to avoid "dead chips"—a specific "beneficial" reason—and ties these teachings specifically to FPGA contact points in the Zavracky-Chiricescu-Akasaka" stack to test memory in that stack. *See* Pet. Reply 19–20 (reiterating five reasons supplied in the Petition, including, for example, "(1) the known problem of the need to test stacked modules to avoid the expense and waste of silicon by creating 'dead' chips" (citing Ex. 1002 ¶ 241 (citing Ex. 1009; Ex. 1020; Ex. 1043); Pet. 41–42 (explaining that "[i]n the Zavracky-Chiricescu-Akasaka-Satoh Combination, the test signal is sent

through the contact points between the FPGA of the first IC die element and the memory of the second IC die element, which is how those elements are stacked and electrically coupled" (citing Ex. 1008, 49:32–37; Ex. 1002 ¶¶ 357–59)).

In other words, Petitioner persuasively shows a reasonable expectation of success with specific reasons to combine, all supported by the record, including beneficial testing to avoid dead chips and maintain reliable memory to reconfigure the 3D stack's FPGA post-manufacture, thereby showing how to apply the teachings to the claimed 3D stack as suggested by Zavracky, Chiricescu, and Akasaka. Specifically, claims 3 and 28 each recites "wherein said contact points are further functional to provide test stimulus from said [FPGA] to said at least second integrated circuit die element." Petitioner persuasively applies Satoh's teachings to these contact points in order to avoid dead chips.

Patent Owner advances an argument in its Sur-reply that "[t]he references Petitioner and Dr. Franzon cite do not disclose testing of 3D stacked processor[s] but instead disclose that individual die[s] are tested independently and prior to any 3D packaging." Sur-reply 15. This argument is not relevant to a claim limitation at issue here. Neither claim 3 nor claim 28 recite packaging, and neither precludes "provid[ing] test stimulus from said field programmable gate array to said at least second integrated circuit die element" prior to any packaging.

Patent Owner cites to a single paragraph of Dr. Souri's declaration that is conclusory. PO Resp. (citing Ex. 2011 ¶ 83); Ex. 2011 ¶ 83 (Dr. Souri testifying without citation to references or explanation). We give

little weight to Dr. Souri's conclusory and unsupported testimony.

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Satoh would have rendered obvious claims 3 and 28.

F. *Asserted Obviousness of Claims 5 and 30*

Petitioner contends claims 5 and 30 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Alexander. Pet. 42–45.

1. *Disclosure of Alexander*

Alexander describes "stacking together a number of 2D FPGA bare dies" to form a 3D FPGA. Ex. 1009, 1.[24] Alexander explains that "each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die." Ex. 1009, 1.

[24] We cite, as Petitioner does, to the exhibit page numbers (rather than to the original page numbers.

Alexander's Figure 2 follows:

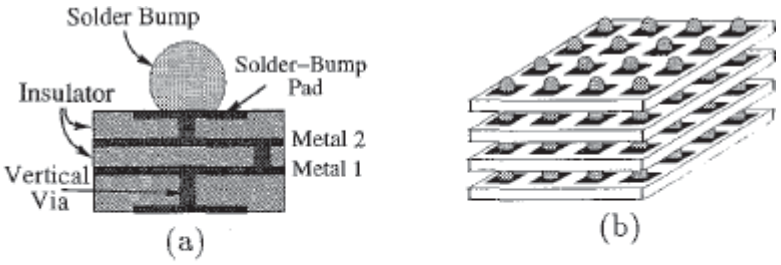


Figure 2: (a) The solder bump, pad, and vertical via geometry; and (b) stacked 2D FPGA dies.

Figure 2(a) shows vertical vias traversing a chip with a solder pad and solder bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1009, 1.

Alexander explains that stacking dies to form a 3D FPGA results in a chip with a "significantly smaller physical space," lower "power consumption," and greater "resource utilization" and "versatility" as compared to conventional layouts. Ex. 1009, 1.

2. *Claims 5 and 30*

Claim 5 depends indirectly from independent claim 2, and claim 30 depends indirectly from independent claim 27. Claims 5 and 30 each further recite "wherein said third integrated circuit functional element includes another field programmable gate array."

a. Petitioner's Combination

For claims 5 and 30, Petitioner relies on a combination of Zavracky, Chiricescu, Akasaka, and Alexander. Pet. 42–45. In reciting "wherein said third

integrated circuit functional element includes another field programmable gate array," claims 5 and 30 each essentially adds another FPGA to claim 27 as addressed above, requiring at least three stacked integrated circuit die elements: a memory array stacked with "another" FPGA (i.e., a total of two FPGAs), with the "integrated circuit functional elements," which "include[]" the memory array and two FPGAS, electrically coupled together by "a number of contact points distributed through the surfaces of said functional elements," "wherein said memory array is functional to accelerate external memory references to said processing element [one of the FPGAs]" (as recited in independent claim 2) or "wherein said memory array is functional to accelerate external memory references to said processing element" (as recited in independent claim 27).

Petitioner relies on Alexander as disclosing "multiple stacked FPGA functional elements in different layers of a 3D package." Pet. 44 (citing Ex. 1009, 1–3, Fig. 2; Ex. 1002 ¶ 321). As such, Petitioner contends that the combination of Zavracky, Chiricescu, Akasaka, and Alexander provides the additional FPGA as required by claims 5 and 30.

Regarding the requisite reason to combine, Petitioner contends as follows:

> [One of ordinary skill in the art] would have known (as Zavracky notes) that multiprocessor systems were needed for "parallel processing applications," for example, "signal processing applications." Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶258. But in this context, [one of ordinary skill in the art] would have appreciated

> Alexander's teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). *Id.* [One of ordinary skill in the art] would have sought out Alexander's multiple stacked FPGAs to enhance the Zavracky-Chiricescu- Akasaka Combination by upgrading it for this type of application. Ex. 1002 ¶259.

Pet. 43.

Additionally, Petitioner asserts one of ordinary skill in the art "would have had a reasonable expectation of success in integrating Alexander into that existing combination." Pet. 43. More specifically, Petitioner contends that Alexander's similar structure—having multiple stacked FPGAs, as similar to multiple processors stacked with multiple memories of the Zavracky-Chiricescu-Akasaka combination—evidences a reasonable expectation of success of stacking FPGAs with memories, "with multiple functional elements stacked and vertically interconnected including using thousands of contact point vias (holes)." Pet. 43–44. Petitioner also asserts that "[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to known methods to yield a predictable result." Pet. 44 (citing Ex. 1002 ¶¶ 260–61).

b. Patent Owner's Contentions

Patent Owner responds that "Petitioner's only rationale for the combination of all four references . . . merely identifies a generalized benefit without

sufficiently linking it to the features of the claimed invention," and so "Petitioner fails to adequately explain how or why Alexander's multiple FPGA dies can and would be combined with Zavracky-Chiricescu-Akasaka to reach the" limitation recited in claims 5 and 30. PO Resp. 42. More specifically, Patent Owner contends that "[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no bearing on whether a POSITA would have been motivated to combine Alexander with Zavracky-Chiricescu-Akasaka to reach a 3-D processor module having 'a third integrated circuit die element [that] includes another field programmable gate array.'" PO Resp. 42–43 (citing Ex. 2011 ¶ 84).

Patent Owner also argues that Petitioner's "conclusory rationale is further discredited by Petitioner's suggestions elsewhere in the Petition that Chiricescu discloses a FPGA application that enhances Zavracky." PO Resp. 43 (citing Pet. 19). More specifically, Patent Owner argues that the Petition elsewhere suggest that a "POSITA would have taken Chiricescu's suggestion of a FPGA to perform 'arbitrary logic functions,' . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in Zavracky, e.g., to perform image and signal processing tasks that would have taken advantage of co-stacked microprocessors and memories as taught in Zavracky." PO Resp. 43 (quoting Pet. 19). Patent Owner argues that "there is no reason . . . to combine Alexander with Zavracky-Chiricescu-Akasaka," because "Petitioner acknowledges that, Chiricescu, like Alexander, offers FPGAs to enhance parallel

processing image and signal tasks of Zavracky's microprocessor." PO Resp. 43 (citing Ex. 2011 ¶ 85).

Patent Owner also contends that Petitioner fails to explain how the combination would be made with a reasonable expectation of success. PO Resp. 43–45. Patent Owner contends that "[n]either Petitioner nor Dr. Franzon provide any analysis of" Alexander's "acknowledgment that '[t]he 3D FPGA model gives rise to a number of new challenges,' including heat dissipation and heat stress (collectively, 'thermal issues')." PO Resp. 44; PO Sur-reply 17–18.

In response to Petitioner's Reply, Patent Owner more specifically contends that Petitioner does not sufficiently explain why or how one of ordinary skill in the art would have combined Alexander's 3D FPGA into the Zavracky-Chiricescu-Akasaka combination when the combination "already includes Chiricescu's FPGA on the first integrated die element and that Alexander's 3D FPGA architecture is disparate from Chiricescu's." PO Sur-reply 16 (reproducing Chiricescu's Fig. 2 "depicting a separate memory, routing, and RLB layers in the FPGA" and Alexander's Fig. 2 "depicting stacked 2D FPGA dies using solder bumps"). Patent Owner argues that Petitioner does not sufficiently address using disparate FPGA architecture in the first and third integrated die elements because Petitioner "fails to explain how the circuitry of Alexander's 3D FPGA would be laid out, connected to, and operating with the proposed Zavracky-Chiricescu-Akasaka structure, which already includes Chiricescu's unique FPGA to arrive at the claimed invention." PO Sur-reply 17.

c. Analysis

We determine that Petitioner provides sufficient evidence supporting Petitioner's asserted reason to combine. Petitioner contended as follows:

> [One of ordinary skill in the art] would have known (as Zavracky notes) that multiprocessor systems were needed for "parallel processing applications," for example, "signal processing applications." Ex. 1003, 12:13–28, Fig. 12; Ex. 1002
>
> ¶258. But in this context, [one of ordinary skill in the art] would have appreciated Alexander's teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). *Id.* [One of ordinary skill in the art] would have sought out Alexander's multiple stacked FPGAs to enhance the Zavracky-Chiricescu- Akasaka Combination by upgrading it for this type of application. Ex. 1002 ¶259.

Pet. 43. Petitioner's evidence includes reasoning provided by Zavracky based on a plain reading of the cited passage. *See, e.g.,* Ex. 1003, 12:13–17 ("This technology is also useful in the microprocessor environment. FIG. 12 presents a stacked microprocessor and random access memory array which is one potential microprocessor embodiment used in parallel processing applications. The first layer 700 is **a microprocessor** which shares random access memory 702 on the second layer, [with] **another microprocessor** 704 located above the random access memory. This configuration lends itself

well to use in signal processing applications." (emphasis added)).

Petitioner's evidence also includes Dr. Franzon's declaration testimony that one of ordinary skill in the art would have used "Alexander's multiple stacked FPGAs to enhance" Petitioner's combination because such stacked FPGA's were preferred because "(1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible)." Pet. 43 (citing Ex. 1002 ¶ 258). We credit Dr. Franzon's testimony that provides well-reasoned explanation and analysis based on quoted passages from a 2000 IEEE article (Ex. 1058) that examined "processors and FPGAs to characterize and compare their computational capabilities" and another reference describing customized parallel hardware. Ex. 1058, 41[25]; Ex. 1051; *see* Ex. 1002 ¶ 258 (quoting Ex. 1058, 43; quoting Ex. 1051, 3:45–67).

In addition, claims 5 and 30 each recite "said third integrated circuit functional element includes another field programmable gate array" (FPGA). Petitioner's arguments and evidence includes Dr. Franzon's testimony that one of ordinary skill in the art would have used "Alexander's multiple stacked FPGAs" because "stacked FPGA's were preferred." Thus, we do not agree with Patent Owner's assertion that "Petitioner's alleged motivation to combine is untethered to the claimed invention." PO Resp. 42–43.

Furthermore, in contrast to Dr. Franzon's well-supported testimony in this regard, Patent Owner's expert, Dr. Souri, in paragraph 84 provides only

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[25] Citation is to original page numbers of article.

conclusory statements. For example, Dr. Souri states, without providing explanation or evidence, "[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no bearing on whether a skilled artisan would have been motivated to combine Alexander with Zavracky-Chiricescu-Akasaka to reach a 3-D processor module having 'a third integrated circuit functional element [that] includes another field programmable gate array.'" Ex. 2011 ¶ 84. The only citations in paragraph 84 are citations to the claims in the challenged patent and to the Petition's assertion that Dr. Souri attempts to rebut. Ex. 2011 ¶ 84 (only citing Ex. 1001, claims 5 and 30; Pet. 43). We give little weight to Dr. Souri's conclusory and unsupported testimony in this regard.

Dr. Souri also testified that "in my opinion there is no reason whatsoever that [one of ordinary skill in the art] would have looked to combine Alexander with Zavracky-Chiricescu-Akasaka" because "Chiricescu, like Alexander, offers FPGAs to enhance parallel processing image and signal tasks of Zavracky's microprocessor." Ex. 2011 ¶ 85. As noted above, however, Dr. Franzon provides specific reasons, supported by evidence and uncontroverted in the record, as to why one of ordinary skill in the art "would have viewed Alexander's teaching of stacked FPGAs as preferable over alternatives" in a multiprocessor system, as Petitioner responds. Pet. Reply 21. Additionally, in Reply, Petitioner cites a patent issued in 1996 that indicates "a stack of 4 FPGA's, for example, would have the potential of being used to performing a digital task having four times the complexity that a single FPGA could perform" that further supports Dr. Franzon's that

processing tasks were further improved when multiple FPGAs were stacked together. Pet. Reply 22 (quoting Ex. 1027, 2:58–60).

For these reasons, we determine that, Petitioner has provided sufficient evidence of a reason why one of ordinary skill in the art would have combined Alexander with the Zavracky-Chiricescu-Akasaka combination.

Contrary to Patent Owner's argument that Petitioner did not describe how to combine the references, Petitioner also indicated in the Petition that "using multiple dies in the stack at taught by Alexander would work in a straightforward manner similar . . . to stacking multiple memories, or multiple microprocessors, as already taught in the Zavracky-Chiricescu- Akasaka Combination." Pet. Reply 21 (quoting Pet. 44). Petitioner continues in the Petition asserting, "[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to known methods to yield a predictable result." Pet. 44 (citing Ex. 1002 ¶¶ 260–61).

The record does not support Patent Owner's assertions that multiple FPGAs would not work in a straightforward manner and one of ordinary skill in the art would not have had a reasonable expectation of success. *See* PO Resp. 43–44. First, Petitioner's combination "simply combin[es] the extra FPGA of Alexander with the existing 3-D stack" of the Zavracky, Chiricescu, and Akasaka combination "according to known methods to yield a predicable result." Pet. 44 (citing Ex. 1002 ¶¶ 260–61). In the words of Dr. Franzon,

> the result of this combination would have been predictable, simply combining the extra FPGA of Alexander . . . with the existing 3-D stack according to known methods (the same methods used to attach the other integrated circuit functional elements) to yield a predictable result (two FPGAs in the stack).

Ex. 1002 ¶ 261. Patent Owner provides no evidence that undermines this persuasive straightforward explanation of how Petitioner proposes to combine Alexander's FPGA in the Zavracky, Chiricescu, and Akasaka combination.

Turning to Patent Owner's assertion based on Alexander's indication of thermal issue challenges and the need to reduce power consumption to mitigate thermal issues (PO Resp. 44), we agree with Petitioner that one of ordinary skill in the art, in view of Zavracky's teaching of a FPGA with a memory and a microprocessor in Figure 13, "would have understood that combining an FPGA with a memory and another FPGA (as in claims 5 and 30) would **reduce** purported thermal issues, not increase them." Pet. Reply 22 (citing Ex. 1003, 12:29–39, Fig. 13; Ex. 1070 ¶¶ 37–41). Petitioner explains that "FPGAs were more energy-efficient than microprocessors for the same size die, reducing heat." Pet. Reply 22–23 (citing Ex. 1070 ¶¶ 37– 41 (citing Ex. 1058, 1082)). We are persuaded by Petitioner's position, which is based on Dr. Franzon's declaration testimony. We credit Dr. Franzon in view of his reasonable explanation and analysis that relies on citations to references that support his testimony. *See* Ex. 1070 ¶¶ 37–41 (citing Ex. 1003, 12:29–39, Fig. 13; Ex. 1058, 43; Ex. 1082).

Petitioner also provides evidence that thermal management was a routine consideration in view of various known ways to address thermal issues. Pet. Reply 23 (citing Ex. 1020, 11 for "describing and citing five 'methods [that] are effective' for thermal management).

For these reasons, we conclude that Petitioner has provided by a preponderance of evidence articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Alexander would have rendered obvious claims 5 and 30.

G. *Exhibit 1070*

Patent Owner argues that "[p]aragraphs 5–9, 13–41, 59–68, 79–89, and 90–103 from Dr. Franzon's second declaration (Ex. 1070)" in reply to Patent Owner's Response are not sufficiently discussed in the Reply. PO Sur-reply 18. Patent Owner contends that "Petitioner provides no substantive discussion of Dr. Franzon's testimony . . . but instead references Dr. Franzon's testimony from the abovementioned paragraphs (collectively spanning over roughly 39 pages) based on citation alone or a cursorily parenthetical." PO Sur-reply 18–19 (identifying Pet. Reply 7, 8, 10, 16, 17,

19, 22, and 23).

Patent Owner contends that "Dr. Franzon's arguments from his second declaration [Reply Declaration] should not be considered." PO Sur- reply 19 (citing 37 C.F.R. § 42.6(a)(3) ("Arguments must not be incorporated by reference from one document into another document."); *Gen. Access Sols., Ltd. v. Sprint Spectrum L.P.*, 811 F. App'x 654, 658 (Fed. Cir. 2020) (standing for "upholding the Board's finding of improper incorporation by reference because, *inter alia*" "'playing archaeologist with the record' is precisely what the rule against incorporation by references was intended to prevent")).

The situation here is different than in *General Access Solutions*, because there, the court noted a problem with identifying a party's substantive arguments *prior to turning to the declaration at issue*: "*To identify GAS's substantive arguments*, the Board was forced to turn to a declaration by Struhsaker, *and further to delve into a twenty-nine-page claim chart attached as an exhibit*." *Gen. Access Sols.*, 811 F. App'x 658 (emphasis added). Here, Patent Owner does not describe or allege any problem with identifying Petitioner's substantive arguments.

In addition, Patent Owner provides a list of Reply Declaration paragraphs and a list of reply pages without identifying with particularity where the identified paragraphs may be found. It appears that not all the paragraphs identified by the Patent Owner are located on any of the identified Reply pages. For example, paragraphs five through nine do not appear to be included in any of the Reply pages identified by Patent Owner. Those paragraphs address the level of ordinary skill in the art. Similarly, Patent Owner

identifies paragraphs 59–68 and, of the identified Reply pages, paragraphs 59–66 are referenced on Reply page 19 and paragraphs 65 and 68 are referenced on Reply page 16. Paragraph 67 does not appear to be referenced on any of the Reply pages identified by Patent Owner.

Even setting aside these discrepancies in Patent Owner's Sur-reply, we do not agree with Patent Owner that we should not consider Dr. Franzon's Reply Declaration. Patent Owner makes only general assertions that seem to be based primarily on multiple paragraphs being identified in a citation, which as discussed below we find provide context for Petitioner's arguments. Additionally, Patent Owner does not address the significant overlap in the cited paragraphs with arguments made in the Reply. Moreover, in reaching our decision regarding the patentability of the challenged claims, we exercised judgment as to all the evidence cited by the parties for its relevance, context, and substance, and weighed it accordingly.

We turn now to each page in the Reply identified by Patent Owner as having improperly incorporated arguments. Regarding Reply page 7, Patent Owner identifies paragraphs 79–89 of the Reply Declaration. These paragraphs provide opinions in response to our claim construction discussion in the Institution Decision and those paragraphs are referenced on page 7 of the Reply in the section asserting that Petitioner's Zavracky, Chiricescu, and Akasaka combination meets the Board's claim interpretation. Paragraphs 83 and 84 discuss Zavracky's inter-layer connections, and are substantially similar to Petitioner's arguments on page 5 of the Reply. Paragraph 85

discusses Chiricescu and is substantially similar to Petitioner's arguments on page 6 of the Reply. Paragraphs 87 and 88 discuss Akasaka and are substantially similar to Petitioner's arguments on pages 6 and 7 of the Reply. Notably, the arguments in this section of the Reply (pages 5–7) principally rely on the express disclosures of the references. Petitioner's reference to paragraphs 79–89 of the Reply Declaration serve to confirm the correctness of Petitioner's understanding of the plain language of the references presented within this section of the Reply.

Petitioner's reference on page 8 of the Reply to paragraphs 90–93 of the Reply Declaration follows a similar pattern. Petitioner on page 8 of the Reply asserts that the Zavracky, Chiricescu, and Akasaka combination increases speed in the same five ways as the challenged patent and identifies five citations to the challenged patent, as does paragraph 91 in the Reply Declaration. The additional three cited paragraphs provide additional context—including two conclusions (paragraphs 90 and 93) and discussion of testimony by another Patent Owner expert (paragraph 91), which was not necessary for our decision regarding patentability.

Page 10 of the Reply cites paragraphs 94–103 of the Reply Declaration in asserting the Zavracky, Chiricescu, and Akasaka combination meets "the functional to accelerate" limitations under Patent Owner's proposed interpretation of what structure the claims require in a wide configuration data port. Pet. Reply 9–10. The Reply Declaration paragraphs 94 and 95 directly address Petitioner's Reply arguments regarding Patent Owner's expert testimony, including

Dr. Chakrabarty[26] regarding the ordinary and custom meaning of a wide configuration data port. including citing substantially the same portions of the relevant deposition transcript as Petitioner in its Reply. Pet. Reply 9 (quoting Ex. 1075, 157:23–158:3); Ex. 1070 ¶¶ 94–95 (citing Ex. 1075, 163–64, 157–58). Paragraph 103 largely overlaps the discussion of Zavracky and Chiricescu on pages 9–10 of the Reply. Petitioner's Reply is ambiguous as to what portions of the Reply Declaration are cited because the Reply Declaration presents paragraphs 94, 95, and 103, and then presents paragraphs 96–102, which address claim limitations in the '226 patent not at issue here. Thus, a reasonable inference is that the Reply citation of 94–103 means the sequential pages that include only paragraphs 94, 95, and 103, which largely mirror Petitioner's arguments on pages 9 and 10 of the Reply.

On page 16 of the Reply, Petitioner cites two paragraphs of the Reply Declaration (65 and 68) with a clear parenthetical explanation ("Dr. Franzon noting the routine use of on-chip area-wide connections in 3D stacks, including his prior work, Ex. 1020").

On page 17 of the Reply, Petitioner cites paragraphs 13–28 with a clear parenthetical explanation ("Dr. Franzon rebutting Dr. Souri's testimony as to each purported issue with citations to

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[26] Dr. Chakrabarty was Patent Owner's expert in IPR2020-01020, IPR2020- 01021, and IPR20220-01020. Exhibit 1071 in this proceeding is Dr. Chakrabarty's deposition in those cases. Petitioner uses Dr. Chakrabarty's deposition testimony here to undermine Patent Owner's position regarding a wide configuration data port. Pet. Reply 9; Ex. 1070 ¶¶ 94–95 (citing Ex. 2011 ¶ 55; citing Ex. 1075, 163–64, 157–58).

evidence."). This supports the prior sentence asserting the "TSV interconnection issues" identified by Patent Owner were "at most normal engineering issues" by asserting that each issue was rebutted by Dr. Franzon. We understand Petitioner in this context to point to these paragraphs, not for the detailed rebuttals, but for the fact that Dr. Franzon analyzed the issues identified by Dr. Souri. Similarly, in note 7 on page 19 of the Reply, Petitioner identifies paragraphs 59–66 in the parenthetical—"Dr. Franzon rebutting Dr. Souri's opinions re: same"—as supporting the assertion that Patent Owner "describes Akasaka's teaching inaccurately." Again on page 23 of the Reply, in the context of Petitioner's contention that thermal issues were a routine consideration, paragraphs 29–41 of Dr. Franzon's Supplemental Declaration are cited with the parenthetical explanation: "Dr. Franzon rebutting Dr. Souri's ipse dixit with evidence of known ways to address thermal issues."

On pages 22 of the Reply, Petitioner references paragraphs 37–41 with a parenthetical explanation: "Dr. Franzon noting that use of a second FPGA die would have reduced any purported thermal issues as compared to a similar stack with a microprocessor." This directly follows and supports Petitioner's contention: "Given this teaching in Zavracky, [one of ordinary skill in the art] would have understood that combining an FPGA with a memory and another FPGA (as in claims 5 and 30) would reduce purported thermal issues, not increase them."

Accordingly, for these reasons, the examination of the citations identified by Patent Owner in full

context, reveals that Petitioner's use of and citation to Dr. Franzon's testimony is not improper.

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.[27] In summary:

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent-able
1, 2, 4, 6, 26, 27, 29, 31	103(a)	Zavracky, Chiricescu, Akasaka	1, 2, 4, 6, 26, 27, 29, 31	
3, 28	103(a)	Zavracky, Chiricescu, Akasaka, Satoh	3, 28	

[27] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent-able
5, 30	103(a)	Zavracky, Chiricescu, Akasaka, Alexander	5, 30	
Overall Outcome			1–6, 26–31	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–6 and 26–31 of the '214 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

APPENDIX E

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case IPR2020-01568[1]
Patent 7,282,951 B2

XILINX, INC., PETITIONER,

v.

ARBOR GLOBAL STRATEGIES, LLC, PATENT OWNER

Entered: Mar. 2, 2022

FINAL WRITTEN DECISION

35 U.S.C. § 318(a)

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, Administrative Patent Judge.

Xilinx, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1, 2, 4–6, and 8–29 (the "challenged claims") of U.S. Patent No. 7,282,951 B2 (Ex. 1001, "the '951 patent"). Petitioner filed a Declaration of Dr. Paul Franzon (Ex.

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[1] Taiwan Semiconductor Manufacturing Co. Ltd. "TSMC" filed a petition in IPR2021-00736, and the Board joined it as a party to this proceeding. *See also* Paper 38 (order dismissing-in-part TSMC as a party with respect to claims 1, 4, 5, 8, 10, and 13–15).

1002) with its Petition. Arbor Global Strategies, LLC ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.").

After the Institution Decision (Paper 12, "Inst. Dec."), Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp.") and a Declaration of Dr. Shoukri J. Souri (Ex. 2011); Petitioner filed a Reply (Paper 22) and a Reply Declaration of Dr. Paul Franzon (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 26, "Sur-reply"). Thereafter, the parties presented oral arguments via a video hearing (Dec. 3, 2021), and the Board entered a transcript into the record. Paper 32 ("Tr.").

For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

Petitioner identifies Xilinx, Inc. as the real party-in-interest. Pet. 68. Patent Owner identifies Arbor Global Strategies LLC. Paper 4, 1. Joined party Taiwan Semiconductor Manufacturing Co. Ltd. is also a real party-in- interest. *See supra* note 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC, v. Xilinx, Inc.*, No. 19-CV-1986-MN (D. Del.) (filed Oct. 18, 2019) as a related infringement action involving the '951 and three related patents, U.S. Patent No. RE42,035 E (the "'035 patent,"), U.S. Patent No. 6,781,226 B2 (the "'226 patent") and U.S. Patent No. 7,126,214 B2 (the "'214 patent"). *See* Pet. 68–69; Paper

4. Petitioner "contemporaneously fil[ed] *inter partes* review (IPR)] petitions challenging claims in each of these patents," namely IPR2020-01567 (challenging the '214 patent), IPR2020-01570 (challenging the '035 patent), and IPR2020-01571 (challenging the '226 patent). *See* Pet. 68. Final written decisions for these three cases issue concurrently with the instant Final Written Decision.

The parties also identify *Arbor Global Strategies LLC* v. *Samsung Electronics Co., Ltd.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) as a related infringement action involving the '035, '951, and '226 patents. *See* Pet. 69; Paper 4. Subsequent to the complaint in this district court case, Samsung Electronics Co., Ltd. ("Samsung") filed petitions challenging the three patents, and the Board instituted on all challenged claims, in IPR2020-01020, IPR2020-01021, and IPR2020-01022. *See* IPR2020-01020, Paper 11 (decision instituting on claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the '035 patent); IPR2020-01021, Paper 11 (decision instituting on claims 1, 4, 5, 8, 10, and 13–15 the '951 patent); IPR2020-01022, Paper 12 (decision instituting on claims 13, 14, 16–23, and 25–30 of the '226 patent).

The Board recently issued final written decisions in the three Samsung cases, determining all challenged claims unpatentable. *See* IPR2020-01020, Paper 30 (holding unpatentable claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29 of the '035 patent); IPR2020-01021, Paper 30 (holding unpatentable claims 1, 4, 5, 8, 10, and 13–15 of the '951 patent); IPR2020-01022, Paper 34 (holding unpatentable claims 13, 14, 16–23, and 25–30 of the '226 patent).

The Board joined Taiwan Semiconductor Manufacturing Co. Ltd. as a party in each of the prior proceedings as it did here.

C. *The '951 patent*

The '951 patent describes a stack of integrated circuit ("IC") die elements including a field programmable gate array ("FPGA") on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '951 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." *Id.*

Figure 4 follows:

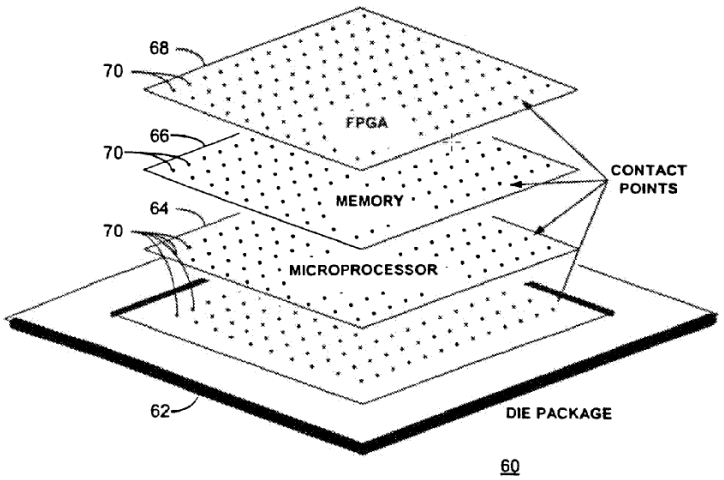

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 68, memory die 66, and microprocessor die 64, interconnected using metal and contact holes 70. Ex. 1001, 4:61–5:8.

The '951 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:26–41. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See id.* Such a "reconfigurable processor" also provides a known benefit of flexibly providing of different logical units required by an application after manufacture or initial use. *See id.*

D. *Illustrative Claim 1*

Independent claim 1 illustrates the challenged claims at issue:

> 1. A processor module comprising:
>
> [1.1] at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and
>
> [1.2] at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element [1.3] wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements and [1.4] wherein said second integrated circuit includes a

memory array functional to accelerate external memory references to the processing element.

Ex. 1001, 7:58–8:4; *see* Pet. 23–30 (addressing claim 1).

E. *The Asserted Grounds*

Petitioner challenges claims 1, 2, 4–6, and 8–29 of the '951 patent on the following grounds (Pet. 1):

Claims Challenged	35 U.S.C. §	References
1, 2, 4–6, 8–24, 27, 29	103[2]	Zavracky,[3] Chiricescu,[4] Akasaka[5]
25	103	Zavracky, Chiricescu, Akasaka, Trimberger[6]
26	103	Zavracky, Chiricescu, Akasaka, Satoh[7]
28	103	Zavracky, Chiricescu, Akasaka, Alexander[8]

II. ANALYSIS

Petitioner challenges claims 1, 2, 4–6, and 8–29 as obvious based on the grounds listed above. Patent Owner disagrees.

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[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of trial, the '951 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

[3] Zavracky et al., US 5,656,548, issued Aug. 12, 1997. Ex. 1003.

[4] Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98. Ex. 1004.

[5] Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Iss. 12, pp. 1703-1714, Dec. 1986, ISSN 0018-9219. Ex. 1005.

A. *Legal Standards*

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

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[6] Steve Trimberger, Dean Carberry, Anders Johnson, and Jennifer Wong, *A Time-Multiplexed FPGA*, Proceedings of the 1997 IEEE International Symposium on Field-Programmable Custom Computing Machines, April 1997, ISBN 0-8186-8159-4. Ex. 1006.

[7] Satoh, PCT App. Pub. No. WO00/62339, published Oct. 19, 2000. Ex. 1008 (English translation).

[8] Michael J. Alexander, James P. Cohoon, Jared L. Colflesh, John Karro, and Gabriel Robins, *Three-Dimensional Field-Programmable Gate Arrays*, Proceedings of Eighth International Application Specific Integrated Circuits Conference, Sept. 1995. Ex. 1009.

B. *Level of Ordinary Skill in the Art*

Relying on the testimony of Dr. Franzon, Petitioner contends that

> [t]he person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '951 patent would have been a person with a Bachelor's Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication.

Pet. 7 (citing Ex. 1002 ¶¶ 58–60).

Relying on the testimony of Dr. Souri, Patent Owner contends that

> [a] person of ordinary skill in the art ("POSITA") around December 5, 2001 (the earliest effective filing date of the '951 Patent) would have had a Bachelor's degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.

PO Resp. 8–9 (citing Ex. 2011 ¶ 37).

We adopt Petitioner's proposed level of ordinary skill in the art as we did in the Institution Decision, because it comports with the teachings of the '951 patent and the asserted prior art. *See* Inst. Dec. 20–21. Patent Owner's proposed level largely overlaps with Petitioner's proposed level. Even if we adopted Patent Owner's proposed level, the outcome would not change.

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b) (2020). Under this standard, which is the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

The parties' arguments raise a claim construction issue regarding "a memory array functional to accelerate external memory," "said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array" as recited respectively in claims 1, 5, and 10. Independent claims 16, 18, and 23 similarly recite "wherein said memory is functional to accelerate external memory references to [the/said] processing element." Neither party provides an explicit construction.

In the Institution Decision, we determined that

> [t]he parties' arguments raise a claim construction issue regarding "a memory array functional to accelerate external memory," "said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array" as recited respectively in claims 1, 5, and 10. Independent claims 16, 18, and 23 similarly recite "wherein said memory is functional to accelerate external memory references to [the/said] processing element." Neither party provides an explicit construction.

Inst. Dec. 21–22. Tracking the institution decision in related IPR2020- 01021 (also challenging the '951 patent), in the Institution Decision here, we preliminarily construed the "'functional to accelerate' limitations [as] requir[ing] a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and processor." Inst. Dec. 25–26. Likewise, in the final written decision in IPR2020-01021 and in co-pending IPR2020-01570, the Board construed these "functional to accelerate" limitations in materially the same manner. *See* IPR2020-01021, Paper 30, 26, Paper 33 (Errata); IPR2020-01570, Paper 40 (final written decision) § II.C.

In particular, the "functional to accelerate" clauses require "a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory array/memory and processing

element/programmable array." *See* IPR2020-01021, Paper 30, 26, Paper 33 (Errata). We herein adopt and incorporate the construction and the rationale supporting it from the final written decision of IPR2020-01021.

Petitioner states that "[e]ven beyond the Board's construction, the Petition shows that the Zavracky-Chiricescu-Akasaka Combination provides the 'memory array . . . accelerate' limitations under ***any*** reasonable construction," "even under [Patent Owner's] flawed construction." Reply 7, 9. Patent Owner states that it "construes all terms in 'accordance with the ordinary and customary meaning of such claim as understood by on of ordinary skill in the art and the prosecution history pertaining to the patent.'" PO Resp. 9 (quoting 37 C.F.R. § 42.100(b)).

Patent Owner argues that "the claims require . . . structure provided ***within the memory array*** (i.e. the wide configuration data port disclosed in the '951 Patent) that is responsible for accelerating the programmable array's accelerated external memory references." PO Resp. 20 (citing Ex. 2011 ¶ 55). However, Patent Owner fails to describe the particular structure of a wide configuration data port (WCDP) within a memory array the challenged claims require under "the ordinary and customary meaning" or otherwise. *See* PO Resp. 19–20. The '951 patent does not describe a WCDP "within the memory array." Figure 5, for example, depicts "VERY WIDE CONFIGURATION DATA PORT" 82, but Figure 5's WCDP is a separate black box from any structure involving memory or memory array. *Compare* Ex. 1001, Fig. 4 (memory die 66 and vias 70), *with id.* at

Fig. 5 (WCDP 82). *See* Ex. 1001, 5:29–49 (describing Figure 5).

Figure 5 follows:

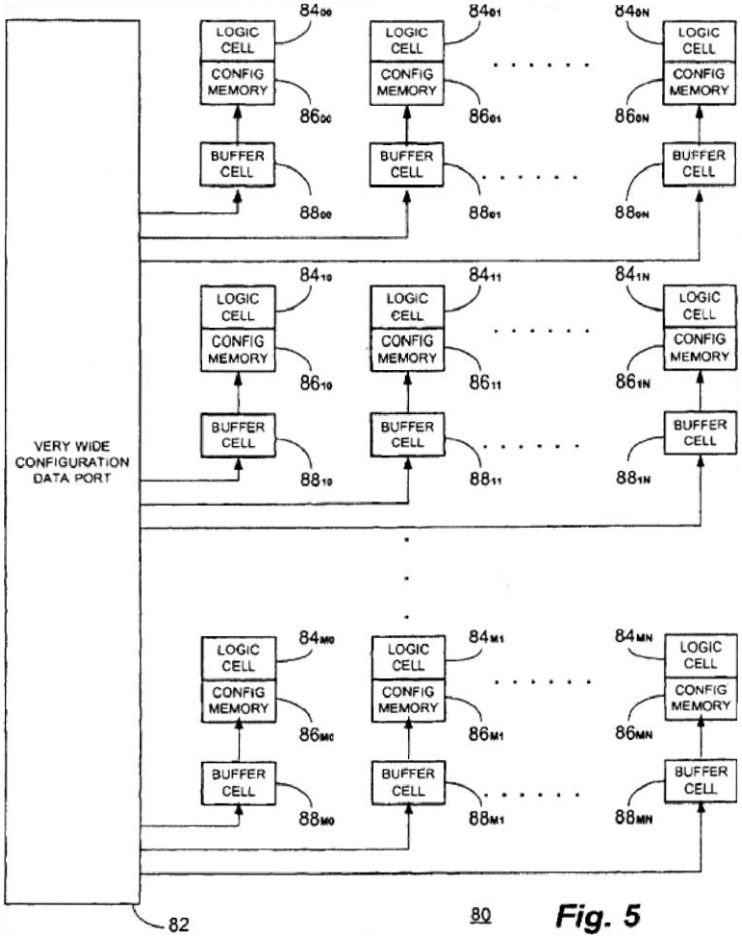

Fig. 5

Figure 5 above illustrates a "VERY" WCDP 82 on the left connected to buffer cells 88, and configuration memory cells 88 and logic cells 84, toward the middle and right. *See* Ex. 1001, Fig. 5; 5:30–49. Buffer cells 88 ("preferably on a portion of the memory die 66" (*see*

Fig. 4)), "can be loaded while the FPGA 68 *comprising the logic cells* 84 *are* [sic] *in operation*." *Id.* at 5:38–42 (emphasis added).[9]

Therefore, the central purpose of the buffer cells is "*they can be loaded while the FPGA 68 comprising the logic cells are in operation*," which "then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it[s] configuration cells 84 updated in parallel." *Id.* at 5:39– 43 (emphasis added). But none of the challenged claims require loading the FPGA while it is in operation. Also, configuration cells and the FPGA can be updated in parallel (e.g., in one clock cycle) without the buffer cells. *See id.*; *see also infra*

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[9] Although the '951 patent states that "[t]he buffer cells 88 are preferably on a portion of the memory die 66 (FIG. 4)" (*id.*) in reference to Figure 5, buffer cells 88 in Figure 5 appear to be near or connected to FPGA logic cells 84 and configuration memory cells 86—perhaps depicting something other than the preferred embodiment describing buffer cells on the memory die. For example, Dr. Chakrabarty testified that the FPGA is to the right of Figure 5's WCDP 82, while memory die 66 (*see* Fig. 4), although undepicted in Figure 5, is to the left of Figure 5's WCDP 82. Ex. 1075, 157:5–158:7; *see also* Reply 9 (quoting 1075, 157:23–158:3). In any event, Figure 5 depicts WCDP 82 as a separate circuit or structure (in black box form) from buffer cells 88 and any memory die or array, and it is not clear how Figure 5's WCDP relates structurally to a memory die or memory array. *See id.* at Fig. 5.

During the Oral Hearing, Patent Owner's arguments further blurred what Figure 5 illustrates. That is, Patent Owner argued that "when the buffer cells are on the FPGA, it then raises the question, okay, well, what's on the memory array, right. And my answer would be *probably* more buffer cells." Tr. 54:21–24 (emphasis added). But there is no disclosure for buffer cells in or on both a memory array and an FPGA die. *See id.* at 55:3–6 (Patent Owner arguing that "I don't think there's anything *that prevents*" buffer cells from being on both dies (emphasis added)).

note 10 (disclosure regarding cache memory providing reconfiguration). Therefore, the challenged claims do not require buffer cells even by implication.

Regardless of the location of the disclosed but unclaimed buffer cells, Figures 4 and 5 and the disclosure indicate that the numerous connections between memory die 66 (with or without buffer cells 88 thereon) and FPGA die 68 (with our without configuration memory cells 86 thereon) facilitate the claimed "functional to accelerate" limitations, in line with our claim construction.[10] In other words, to the extent the claims implicate a WCDP, it is the numerous via connections associated with that port connected to a memory or memory array that support the "functional to accelerate" limitations as discussed further below.

Patent Owner correctly notes that "the '951 Patent discloses that loading configuration data through a typical, relatively narrow [i.e., 8 'bit' or single 'byte'] configuration data port [with respect to prior art Figure 3] led to unacceptably long reconfiguration times." *See* PO Resp. 20 (citing Ex. 1001, 4:47–60); Ex. 1001, 4:54–60 ("Configuration data is loaded through a configuration data port in a *byte serial* fashion and must configure the cells

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[10] The '951 patent implies that configuration memory cells 66 are on FPGA die 68 in one embodiment, but a cache memory provides reconfiguration without them in other embodiments. *See* Ex. 1001, 5:43–50 (stating that "[o]ther methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory ('RAM') than can be offered within the FPGA die itself").

sequentially progressing through the entire array of logic cells 54 and associated configuration memory. It is the loading of this data through a relatively narrow, for example, *8 bit port* that results in the long reconfiguration times." (emphasis added)).[11] Patent Owner contends that "[t]he inventors solved this problem not only by stacking a memory die with a programmable array die, but also by *interconnecting those two elements* with a 'wide configuration data port' that employs through-silicon contacts, with the potential for even further acceleration where the memory die is 'tri- ported.'" *Id.* (citing Ex. 1001, 5:18–25) (emphasis added). This argument itself (which mimics the testimony of Dr. Souri (Ex. 2011 ¶ 56)) shows that any structure associated with the WCDP implicated here simply "interconnect[s] those two [die] elements"—i.e., implicating the numerous vias/contacts 70 as depicted in Figure 4 that connect die elements 66, 66, and 68 together. Therefore, Patent Owner's argument and Dr. Souri's testimony support our analysis and claim construction.

In addressing Petitioner's allegation of obviousness, Patent Owner argues that Petitioner "does not account for all aspects of the claimed

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[11] This description indicates that 8 bits of the single byte load in parallel to the first 8 bit locations of configuration memory 56, and then in succession (serial) to the other 8 bit configuration memory cells. In other words, the quoted description about "byte serial" loading and Figure 3 together show that each byte (i.e., 8 bits) loads over a parallel bus into 8 bit blocks (i.e., a byte) of configuration memory cells in succession (i.e., series). *See* Ex. 1001, Fig. 3 (showing 8 bit configuration data port 52 connected by a bus to a block configuration memory cells 56_{M0} and then in serial to successive blocks of configuration memory cells 56_{M1}–56_{00}).

invention," and states "[f]or example, . . . the '951 patent . . . discloses utilizing a portion of the memory array as a wide configuration data port including buffer cells." PO Resp. 22 (citing Ex. 1001, 5:34–39). This argument for "buffer cells" differs from Patent Owner's argument on page 20 of its Response, which does not mention "buffer cells" and only mentions a "wide configuration data port" as "responsible for accelerating the programmable array's accelerated external memory references." Again, the argument does not explain how the '951 patent shows "utilizing a portion of the memory array as a wide configuration data port."

Based on the specification and claim language as discussed above and further below, apart from numerous vias 70 as depicted in Figure 4, none of the "functional to accelerate" clauses at issue here require any structure associated with a WCDP beyond that included in our construction. In support of our claim construction, Figure 4 of the '951 patent, depicted

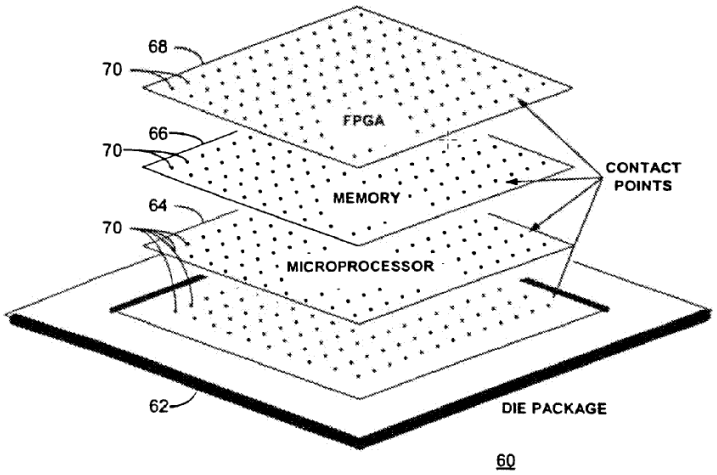

Fig. 4

next, illustrates vias 70 throughout each die, 64, 66, and 68:

As depicted above, Figure 4 shows a number of vias 70 throughout the periphery of each die (i.e., microprocessor die 64, memory die 66, and FPGA 68 die). According to the abstract as quoted above, these "contacts [i.e., vias] . . . traverse the thickness of the die. The processor module disclosed allows for a *significant acceleration* in the sharing of data between the microprocessor and the FPGA element . . . ." Ex. 1001, code (57) (emphasis added). This description of "*significant acceleration*" does not mention a WCDP or buffer cells.

Moreover, the '951 patent specification consistently ties data acceleration to stacking techniques that include vias throughout the stacked dies without requiring other structure. In addition to the abstract, the '951 patent describes "taking advantage of the significantly increased number of connections to the cache memory die." Ex. 1001, 5:44–46. It describes "an FPGA module that uses *stacking techniques* to combine it with a memory die for the purpose of *accelerating* FPGA *reconfiguration*." *Id.* at 2:64–65 (emphasis added). Similarly, it states that "the FPGA module may employ *stacking techniques* to combine it with a memory die *for the purpose of accelerating external memory references*." *Id.* at 2:65–3:2 (emphasis added). The stacking techniques include and refer to the short multiple through-via interconnections 70 *distributed throughout the dies* as depicted in Figure 4. *Id.* at 2:41–46 ("[S]ince these differing die do not require wire bonding to interconnect, it is now also possible to place

interconnect pads throughout the total area of the various die rather than just around their periphery. This then allows for many more connections between the die than could be achieved with any other known technique.").

The '951 patent also explains that "[b]ecause the various die 64, 66 and 68 (FIG. 4) have *very short electrical paths* between them, the signal levels can be reduced while at the same time *the interconnect clock speeds can be increased*." Ex. 1001, 5:53–56 (emphasis added). Similarly, "there is an added benefit of . . . *increased operational bandwidth*." *Id.* at 5:50–53 (emphasis added). As summarized here, these descriptions of shorter electrical paths, increased speed and bandwidth (leading to data acceleration), and acceleration in general, all because of the disclosed stacking techniques (which include multiple short through-vias), apply generally to such speed increases (i.e., acceleration) in the context of Figure 4 without mention of Figure 5's WCDP and buffer cell embodiment, or any tri-port structure. As noted above, even reconfiguration may occur without the specific black box WCDP embodiment of Figure 5, for example, "[o]ther methods for *taking advantage of the significantly increased number of connections* to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68." *Id.* at 5:43–47 (emphasis added); *see also supra* note 10.

Based on the arguments and evidence of record, no reason exists to depart from the claim construction set forth in the final written decision in IPR2020-01021. As Petitioner also argues, Patent Owner did not assert a clear requirement for a WCDP and/or

buffer cells for the "functional to accelerate" clauses in related district court litigation. *See* Reply 2–3 (arguing that Patent Owner does not justify incorporating limitations from the specification and "has taken five inconsistent positions on the 'accelerate' terms across co-pending IPRs and litigations") (citing Ex. 1071 (district court claim chart)); Ex. 1071 (listing various claim construction statements by Patent Owner); Ex. 1072, 27). For example, in the district court litigation, Patent Owner argued as follows:

> The specification teaches *in several sections* that *the short interconnects to the memory die allows for accelerated external memory references*, providing additional context for a POSITA to interpret the claims. Darveaux Decl., ¶ 35. For example, the '951 Patent states that in reference to Figures 4 and 5 that *acceleration* to external memory *is performed because "the FPGA module may employ stacking techniques to combine it with a memory die for accelerating external memory references as well as to expand its on chip block memory*." Ex. 2, '951 Patent at Figs. 4 and 5, 2:56-3:2 (emphasis added).

Ex. 1072, 29 (emphasis added).

In other words, this passage shows that Patent Owner argued in the district court that "short interconnects" of the disclosed "stacking techniques" improve the speed relative to the prior art—without relying specifically on a WCDP, buffer cells, or parallel processing. *See id.* Therefore, contrary to arguments in the Sur-reply, even though Patent Owner advanced other arguments during the district court litigation, none are clear enough to overcome

Patent Owner's broad statements in the district court litigation as quoted above, and Patent Owner has not "taken consistent positions across all IPRs and litigations." *See* Sur-reply 2.

As the Board also preliminarily determined in the Institution Decision, prosecution history of the '951 patent application also plays an important role in understanding the claims and supports the preliminary claim construction. *See* Inst. Dec. 24–25; *accord* Ex. 2006 (institution decision in IPR2020-01021), 24–25. The prosecution history of the '951 patent application further supports our construction.

Specifically, the Examiner indicated allowance of dependent claim 35 of the '951 patent (if written in independent form) over Lin (U.S. Patent No. 6,451,626 B1 (Ex. 1054; Ex. 1107, 67)), finding Lin does not teach or suggest "wherein said memory array is functional to accelerate external memory references to said processing element." Ex. 1107, 72– 73; Inst. Dec. 24–25.

Noting this in our Institution Decision, we pointed to petitioner Samsung's annotation in the IPR1020-01021 proceeding of the following figures from Lin to illustrate the issue:

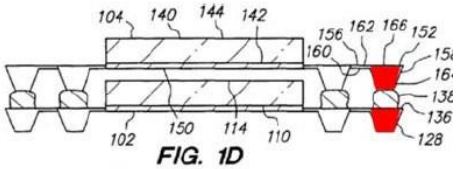

FIG. 1D

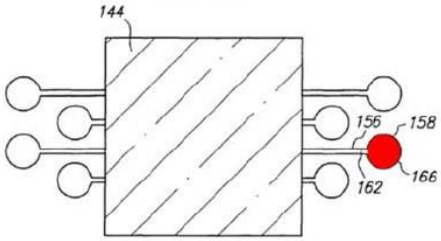

FIG. 2D

Ex. 2006, 25; Inst. Dec. 25. Lin's annotated Figures 1D and 2D above show that Lin discloses contacts (red) on the sides of dies, instead of a number contact vias extending throughout the area of each die within the periphery thereof, in line with the Examiner's reasons for allowance. *See id.*; Ex. 1054 (Lin), Figs. 1D, 2D; Ex. 1107, 72–73.

> Accordingly, as we noted in the Institution Decision,
>
> in light of Lin's teachings and absent explicit explanation during prosecution by the Examiner, the rejection and reasons for allowance provide further support the understanding that the "functional to accelerate" limitations require a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and process[ing element].

Inst. Dec. 25–26; *compare*, Ex. 1001, Fig. 4 (showing numerous contact points), *with* Ex. 1054, Figs. 1D, 2D (showing peripheral contact points).

During the Oral Hearing, Patent Owner argued that with respect to a WCDP that "[*t]he spec is very clear that what we're talking about is it has enough connections to allow the parallel updating of data.*" Tr. 48:20–22 (emphasis added). When asked to compare the '951 patent's Figure 3 (which depicts a prior art eight bit configuration data port) and Figure 5 (which depicts a WCDP), Patent Owner stated that the WCDP "could be as small as 32 bits . . . if you have a small FPGA, right? If you want to update something in parallel, you could update 32-bit with 32 bits?" Tr. 49:1–9 (answering "yes, . . . if you have a very, . . . small FPGA, the number of bits can be . . . relatively smaller, but what's critical is not the number of bits and . . . . [i]t's not necessarily the number of bits that's in the configuration data port, but how they're arranged"). Patent Owner continued by answering that "parallel connections between cells on the die. . . . get to the heart of what the wide configuration data port is, how it works, and how the interconnections between the die work even absent . . . the data being used to configure the FPGA." *Id.* at 49:11–16. Then, Patent Owner argued that "*we all agree* that the wide configuration data port *at least includes these interconnections between the die*. So, what we're talking about is *moving data from one die to another. That's the use of the wide configuration data port*." *Id.* at 49:22–50:2 (emphasis added).

These arguments support our construction because our construction "at least includes these interconnections between the die" and allows data

movement between dies. In addition, contrary to Patent Owner's arguments in the Sur-reply, our construction implicitly distinguishes over the small number of connections in the narrow configuration data port of the '951 patent's prior art Figure 3. *See* Sur-reply 8 (arguing that "Petitioner's . . . interpretation of the wide configuration data port as simply meaning 'a data port used for configuration . . . .[with] a lot of connections though these TSVs' [through silicon vias] . . . . directly contradict[s] the specification [and] . . . also encompasses the conventional 'data port,' which the '951 Patent distinguishes the wide configuration data port from" (quoting Reply 8).

In other words, the "functional to accelerate" clauses require "a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array." *See* IPR2020-01021, Paper 30, 26, Paper 33 (Errata). This construction implicitly represents more vias than prior art Figure 3 of the '951 patent describes (i.e., eight), as supported in view of the specification and prosecution history of the '951 patent. *See* Ex. 1001, Fig. 3 ("8 BIT CONFIGURATION DATA PORT 52"). In addition, as discussed further below and as Petitioner shows, to the extent any of the "functional to accelerate" claims implicate parallel data transfer, our claim construction *allows for* such parallel data transfers—in line with Patent Owner's arguments. *See* Tr. 49:13–16 (Patent Owner arguing that "parallel connections between cells on the die . . . . get to the heart of what the wide

configuration data port is, how it works, and how the interconnections between the die work"); Sur-reply 2 (arguing that "the novel die-area interconnection arrangement with buffer cells (i.e., wide configuration data port) *allows the parallel loading of data* from the memory die to the programmable array that is responsible for the claimed acceleration" (emphasis added)).

Moreover, Patent Owner concedes that "[t]he '951 Patent makes clear that stacking die and short interconnections are simply 'added benefits' that allow for *increased operational bandwidth and speed*." Sur-reply 6 (citing Ex. 1001, 5:51–66) (emphasis added). But increased speed is acceleration—not merely "an added benefit." So is increased bandwidth in context to the '951 patent, because both benefits of *increase in speed* and bandwidth fall within the "functional to accelerate" limitations at issue here for the reasons discussed above. *See* Ex. 1001, 5:30–50; Tr. 56:11–14 (Patent Owner arguing that "[i]f you have a data port that connects in parallel the cells in the memory array with the FPGA cells, that does massively increase bandwidth. . . . but just increasing bandwidth doesn't get you parallel connections"). As noted, our claim construction allows for parallel data transfers (i.e., "a number of vertical contacts distributed throughout . . . to allow multiple short paths for data transfer") so that an increase in bandwidth due to such multiple paths (vias and connections) both satisfies and supports the "functional to accelerate" clauses.

Therefore, as indicated above, we construe the "functional to accelerate" limitations as "a number

of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array."

Based on the current record, no other terms require explicit construction. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy' " (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness, Claims 1, 2, 4–6, 8–24, 27, 29*

Petitioner contends the subject matter of claims 1, 2, 4–6, 8–24, 27, and 29 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 18–52. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 27–44.

1. *Zavracky*

Zavracky, titled "Method for Forming Three Dimensional Processor Using Transferred Thin Film Circuits," describes "[a] multi-layered structure" including a "microprocessor . . . configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure." Ex. 1003, codes (53), (57). Zavracky's "invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing." *Id.* at 2:5–10. Zavracky

includes numerous types of stacked elements, including "programmable logic device[s]" stacked with "memory" and "microprocessor[s]." *See id.* at 5:19–23.

Zavracky's Figure 12 follows:

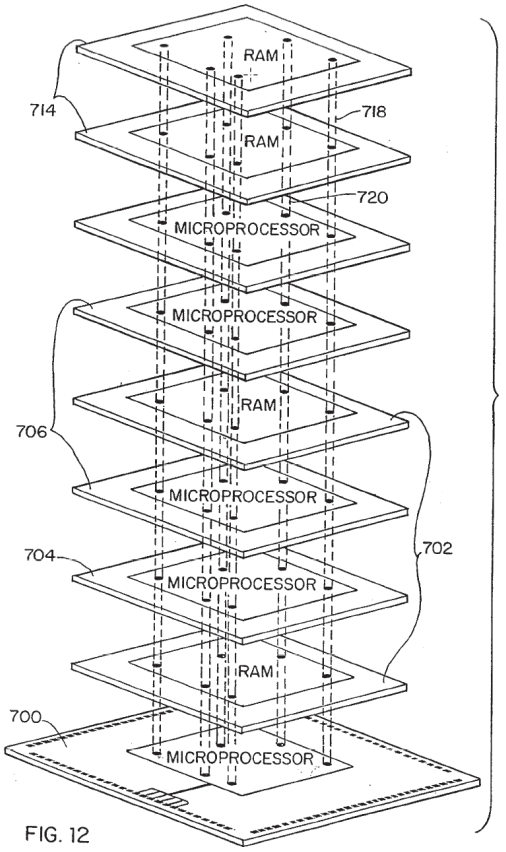

FIG. 12

Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements wherein "buses run vertically through the stack by the use of inter-layer connectors." Ex. 1003, 12:24–26.

2. *Chiricescu*

Chiricescu, titled "A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data," describes a three- dimensional chip, comprising an FPGA layer, memory layer, and routing layer. Ex. 1004, II-232. Chiricescu's FPGA includes a "layer of on-chip random access memory . . . to store configuration information." *Id.* Chiricescu describes and cites the published patent application that corresponds to Zavracky (Ex. 1003) as follows:

> At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.

See id. at II-232, II-235 (citing "P. Zavracky, M. Zavracky, D-P Vu and B. Dingle, '*Three Dimensional Processor using Transferred Thin Film Circuits*,' US Patent Application # 08-531-177, allowed January 8, 1997").[12]

Chiricescu describes "[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information." Ex. 1004, II-232. Chiricescu also describes using memory on-chip to "significantly improve[] the reconfiguration time," explaining as follows:

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[12] Zavracky lists the same four inventors and "Appl. No. 531,177," which corresponds to the application number cited by Chiricescu ("08-531-177"). Ex. 1003, codes (75), (21).

> The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to manage cache memory can be used to administer the configuration data.

Id. at II-234.

Figure 2 of Chiricescu follows:

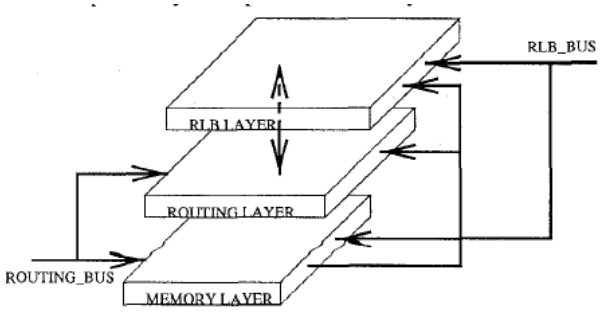

Figure 2. The layers of our 3-D FPGA architecture.

Chiricescu's Figure 2 above illustrates three layers in the 3-D-FPGA architecture, with a "routing and logic blocks" (RLB) layer arranged in a "sea-of-gates FPGA structure," a routing layer, and the aforementioned memory layer (to program/reconfigure the FPGA). *See* Ex. 1004, II-232–233. "[E]ach RLB is connected with the switch-boxes . . . in the routing layer (RL) by means of inter-layer vias. Each RLB can be configured to implement a D-type register and an arbitrary logic function of up to three variables." *Id.* at II-232. Figure 2 also depicts an external ROUTING_BUS to access the 3-D structure with external circuitry to provide configuration data.

Id. at II-232 ("A routing bus provides the configuration information of the routing layer . . . .").

3. *Akasaka*

Akasaka, titled "Three-Dimensional IC Trends" (1986), generally describes trends (several years before the 2001 effective filing date of the invention) in three-dimensional integrated stacked active layers. Ex. 1005, 1703. Akasaka states that "tens of thousands of via holes" allow for parallel processing in stacked 3-D chips, and the "via holes in 3-D ICs" decrease the interconnection length between IC die elements so that "the signal processing speed of the system will be greatly improved." *Id.* at 1705. Akasaka further explains that "[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing" so that "twice the operating speed is possible in the best case of 3-D ICs." *Id.*

Also, "input and output circuits . . . consume high electrical power." Ex. 1005, 1705. However, "a 10-layer 3-D IC needs only one set of I/O circuits," so "power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs." *Id.*

Figure 4 of Akasaka follows:

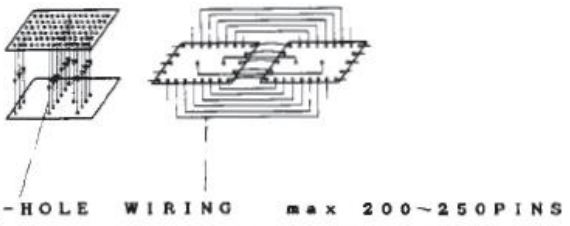

Fig. 4. Wiring for parallel processing in 2-D and 3-D ICs.

Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

According to Akasaka, "[p]arallel processing is expected to be realized more easily in 3-D structures. Several thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or *vice versa*) through them." Ex. 1005, 1705. As one example, Akasaka describes one 3-D chip as including "a video sensor on the top layer, then an A/D converter, ALU [(arithmetic logic unit)], memory, and CPU in the lower layers to realize and intelligent image processor in a multilayered 3-D structure." *Id.*

4. *Petitioner's Showing, Claims 1, 2, 4–6, 8–16, 23, 27, and 29*

Claim 1's preamble recites "[a] processor module comprising." Petitioner relies on the combined teachings of Zavracky, Chiricescu, and Akasaka, as discussed below, and provides evidence that Zavracky discloses a processor module, including a programmable array, memory (RAM), and microprocessor as part of a layered stack forming a 3-D device. *See* Pet. 23 (reproducing Ex. 1003, 5:19–20, 5:21–23, 12:12–38, Figs. 12–13; citing Ex. 1002 ¶¶ 282–288). Zavracky states that "[e]ach circuit layer can be fabricated in a separate wafer . . . and then transferred onto the layered structure and interconnected." Ex. 1003, code (57).

Claim 1 recites limitation [1.1], "at least a first integrated circuit element including a programmable array that is programmable as a processing element."

See Pet. 24. Petitioner contends that the combined teachings of Zavracky and Chiricescu render the limitation obvious. *Id.* Petitioner relies on Zavracky's "programmable logic array 802," and notes that Zavracky states "[t]he array can be formed in any of the layers of a multilayer structure as described elsewhere herein." *Id.* at 25 (quoting Ex. 1003, 12:28–38).[13] Even if Zavracky does not disclose "a programmable array . . . programmable as a processing element," Petitioner contends that "Chiricescu teaches reconfiguring the FPGA as such a processing element wherein the 'FPGA is reconfigured from performing AxB to AxC or vice versa.'" *Id.* at 26–27 (quoting Ex. 1002 ¶ 303 (citing Ex. 1004, 234 (the "example shown is the multiplication of a 4-bit variable")). Petitioner contends that adding such logic to an FPGA would have been obvious because it can be "quickly reconfigured" according to one of Chiricescu's key features. *See id.* at 26 (citing Ex. 1004, II-233–34).

Petitioner also contends that in view of Akasaka, it would have been obvious to modify Zavracky's programmable array to perform different types of processing, including math calculations, signal processing, or image processing. *Id.* at 27 (citing Ex. 1005, 1704–05, 1707, 1709; Ex. 1002 ¶¶ 229, 235

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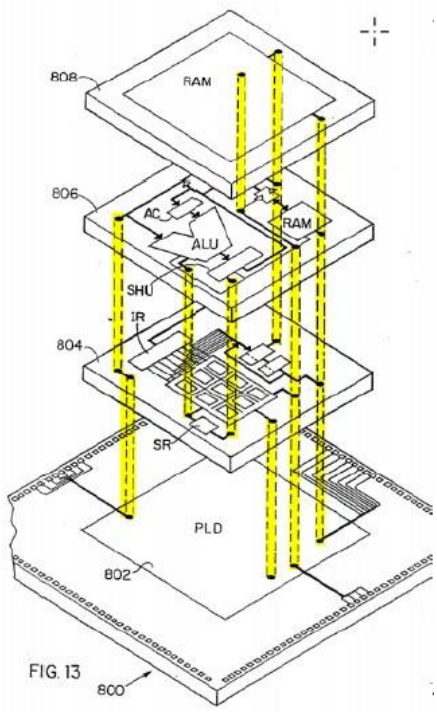
[13] Referring to its analysis of claim 2, Petitioner contends that "the POSITA would have understood Zavracky to be describing a programmable array called a field **programmable** gate **array** (F**P**G**A**), which provides the programmable array element." *See* Pet. 25 n.2 (citing Ex. 1002 ¶¶ 293– 299), 34 (contending, *inter alia*, that "Chiricescu literally describes Zavracky as teaching technology 'to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.'" (quoting Ex. 1004, II-232)).

(citing Ex. 1048; Ex. 1021)). Petitioner adds that an artisan or ordinary skill would have been motivated to employ Akasaka's teachings with Zavracky's stacks for various reasons, including predictably providing multiple distributed contact points and parallel processing to implement a common data memory and cache memory system, and generally to increase bandwidth and processing speed. *See id.* at 20–22 (citing Ex. 1002 ¶¶ 233, 235, 237–239; Ex. 1005, 1705, 1713, Fig. 25).

Claim 1 recites elements [1.2] "at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element" and [1.3]: "wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements."

Petitioner's annotated version of Zavracky's Figure 13 depicts stacked functional elements and the coupled contact points relied upon by Petitioner (Pet. 28):



Zavracky's Figure 13 above as annotated by Petitioner portrays (highlighted) inter-layer via connections (buses), one or more second integrated circuit (IC) functional elements (memory 808 (RAM) die, and microprocessor dies 804 and 806), stacked with "programmable logic array 802." *See* Pet. 27–29.

Petitioner provides evidence that "Zavracky teaches that 'openings or via holes'. . . 'can be placed anywhere on the die' of various functional elements, such that the connections 'are not limited to placement on the outer periphery'." *See* Pet. 30–31 (quoting or citing Ex. 1003, 6:43–47, 13:43–46, 14:56–63).

Petitioner quotes Zavracky as teaching vertically stacked and interconnected circuit element layers:

> One significant aspect in the formation of three-dimensional circuits involves interconnecting the layered devices. . . . Via holes are formed through the upper contact areas to gain access to the lower contact areas. . . . **Electrical contact** between the upper and lower devices is made by filling the via holes 1022 with an electrically conductive material . . . [.]

Pet. 28 (quoting Ex. 1003, 14:51–63). Petitioner points to Zavracky's teaching that "[i]nstead of running buses along the surface of the wafer, many of these run in a vertical direction (the third dimension) between functional blocks freeing up significant real estate for active circuitry." *See id.* (quoting Ex. 1003, 2:48–53).

Petitioner relies on similar teachings in Akasaka: "Akasaka further teaches the contact points are distributed throughout the surfaces of said functional elements, including through the 'tens of thousands of via holes.'" Pet. 31 (quoting Ex. 1004, 1705). Petitioner quotes Akasaka: "Several thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or vice versa) through them." *Id.* at 30 (quoting Ex. 1004, 1705). Petitioner further notes that in Akasaka, "[t]he contact points on the surface of the IC functional elements are created by 'etching [the] via holes.'" *Id.* (citing Ex. 1004, 1707; citing Ex. 1002 ¶¶ 327–332).

Petitioner provides several reasons to combine the reference teachings to suggest providing numerous via holes between stacked dies or chips. *See* Pet. 18–22. As an example, Petitioner points out that Akasaka teaches that "tens of thousands of via holes'

permit parallel processing, and that use of the 'via holes in 3-D ICs' *shortens the interconnection length* between IC die elements so that 'the *signal processing speed of the system will be greatly improved*.'" *Id.* at 18 (emphasis added) (quoting Ex. 1004, 1705).

Petitioner also points out that "Chiricescu . . . explicitly references and uses the interconnections of Zavracky." Pet. 18–19 (*see supra* § II.D.2 (noting the explicit citation to and description of Zavracky in Chiricescu)). Petitioner contends that an artisan of ordinary skill would have understood that combining Zavracky's electrically coupled stacked dies with Chiricescu's teachings of stacked memory for reconfiguring the FPGA (*see* limitation [1.4] below) would significantly improve the reconfiguration time of the FPGA. *See id.* at 18 (citing Ex. 1002 ¶¶ 221–228; Ex. 1004, II-234; Ex. 1003, 5:65–66; Ex. 1020, 2; Ex. 1055 ¶ 14; Ex. 1040, 317). Petitioner adds that an artisan of ordinary skill would have enhanced and expanded Zavracky's programmable logic device within its co-stacked microprocessors and memories to include image and signal processing tasks as Chiricescu's suggests by teaching the use of FPGAs to implement arbitrary logic functions. *See id.* at 19 (citing Ex. 1002 ¶¶ 229–30; Ex. 1005, 1705; Ex. 1003, 12:25–30; Ex. 1004, II-232; Ex. 1058, 41; Ex. 1048).

Petitioner also contends that it was "a predictable advantage and also suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3-D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity." Pet. 20 (citing Ex. 1002 ¶¶ 233; Ex. 1005, 1705). Petitioner adds that "Zavracky and Chiricescu . . . invited such a

combination." *Id.* (citing Ex. 1003, 6:43–47 ("connections . . . can be placed anywhere on the die"); Ex. 1004, 232 (similar)).

> Petitioner further reasons as follows:
>
> the POSITA knew of the need for replicated "common data memory" in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence. Ex. 1002 ¶236 (citing Ex. 1034, 466–469; Ex. 1005, 1713 & Fig. 25). *That structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky*. Ex. 1002 ¶237. A POSITA thus would have been motivated to seek out Akasaka's distributed contact points in order to build a "common data memory." The POSITA's background knowledge, including prior art successes, would have suggested success in this combination. *Id.* (citing Ex. 1005, Ex. 1021).

Pet. 21 (emphasis added). At the cited passage of Dr. Franzon's declaration, Dr. Franzon further explains that the common data memory "still obtain[s] the speed and cost advantages of having an FPGA-based stack (e.g., the FPGA being faster than the software running on a microprocessor, and cheaper than an ASIC)." Ex. 1002 ¶ 237.[14] Dr. Franzon also explains that "the POSITA would have known that the more densely connected communication structure of

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[14] In addition to speed, Dr. Franzon explains that the common data memory employs multi-processor cache coherence in a stacked memory processor design as Akasaka discloses to ensure each shared memory obtains the same updated data that the system broadcasts over the parallel bus. *See* Ex. 1002 ¶ 236 (discussing Ex. 1005, 1713, Fig. 25; citing Ex. 1034, 466–469).

Akasaka would enable desirable uses of the Zavracky-Chiricescu 3D chip stack." *Id.* ¶ 236.

Claim 1 also recites limitation [1.4]: "wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element." Petitioner relies partly on its showings above with respect to the second integrated circuit in limitations [1.2] and [1.3], which include Zavracky's memory array in the stack connected via multiple via connection points. *See* Pet. 32 (citing Ex. 1003, 11:63–65 (("memory may be stacked on top of the multi-layer microprocessor."), 12:15–28 ("random access memory array [with] buses run vertical through the stack"), 12:33–35, Figs. 10, 12, 13 (showing RAM memory 808)).

Petitioner adds the RAM "cache memory" array teachings from Chiricescu further to address the acceleration limitation in limitation [1.4]:

> Chiricescu observes that "[t]he main bottleneck in the implementation of a high performance configurable computing machine is the high configuration time of an FPGA." Ex. 1004 at II-232. This bottlenecking problem is caused in part by having to load configuration data from off-chip memory. Chiricescu's proposed solution used a "memory layer" where the "random access memory is provided to store configuration information." Ex. 1004 at II-232. Rather than having to go "off-chip" each time to load the FPGA reconfiguration data (i.e., load such external memory references each time the data is referenced), Chiricescu's random access memory (i.e., a memory array) acts as a "cache memory" for that reconfiguration data, accelerating access

> to those external memory references. Ex. 1004, II-234. Therefore, when the FPGA (i.e., the processing element) needs to be reconfigured with new data, access to that data is accelerated by already having been loaded into the memory array. Ex. 1004, II-234. Therefore, the Zavracky-Chiricescu- Akasaka Combination, which includes Chiricescu's FPGA and memory, provides this claim element. Ex. 1002 ¶¶304–307.

Pet. 32–33. As summarized above, Petitioner relies on multiple reasons for combining the references, including to increase processing speed by stacking chips with multiple parallel via connections to allow for parallel processing. *See* Pet. 8–9 (citing Bertin (Ex. 1025) as teaching "a stack of chips . . . to minimize latency between the device and chips and to maximize bandwidth" (citing Ex. 1025, 7:18–22, Fig. 22; Ex. 1001 ¶¶ 41–43), 12 ("It was well known that 'interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems,' and that 'wide buses are very desirable' and were made possible by 3-D stacking." (citing Ex. 1020, 2–3; Ex. 1002 ¶¶ 53–57)), 18 ("Akasaka further explains that 'shorter interconnection delay time and parallel processing' means that the processing of data between layers is accelerated such that "twice the operating speed is possible in the best case of 3-D ICs." (quoting Ex. 1005, 1705)), 20 ("[I]t was a predictable advantage and also suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity." (citing Ex. 1002 ¶ 233 as quoting Ex. 1005, 1705)),18–22 (listing

other reasons to combine), 60 ("The POSITA would have known (as Zavracky notes) that multiprocessor systems were needed for 'parallel processing applications,' for example, 'signal processing applications.'" (citing Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶ 258)).

Claim 2 depends from claim 1 and recites "[t]he processor module of claim 1 wherein said programmable array of said first integrated circuit die element comprises an FPGA." Petitioner generally refers to the "[t]he Zavracky-Chiricescu-Akasaka Combination" as it does for claim 1. *See* Pet. 34–35. Citing the testimony of Dr. Franzon and other evidence, Petitioner relies on Zavracky's PLD (programmable logic device) 802 at the bottom of the stack in Figure 13 as an FPGA. *Id.* at 29–31 (citing Ex. 1002 ¶¶ 292–297; Ex. 1035, 1:29–30; Ex. 1036, 4:1–9; Ex. 1037, 1:13–22; Ex. 1038, code (57) (describing "transistors of a programmable logic device (PLD), such as a field programmable gate array (FPGA)").

Petitioner relies on other teachings, including Chiricescu's teachings, including its "sea-of-gates" FPGA layer, and the knowledge of an artisan of ordinary skill, to show that Zavracky's PLD is or at least suggests an FPGA based on Chiricescu's teachings. *See* Pet. 30–31 (citing 1002 ¶¶ 294–297; Ex. 1004, II-232; Ex. 1040; Ex. 1051). Petitioner also generally relies on reasons for combining the references as outlined above with respect to claim 1 to suggest modifying Zavracky's 3-D stack (memory, processor, FPGA) based on Chiricescu's layer/stack teachings (FPGA, memory). *See id.* at 34– 35 (citing Pet. §§ VII.A.2, A.4). Petitioner also notes that

Chiricescu specifically describes Zavracky's teachings (*see supra* § II.D.2) as useful for providing 3-D FPGA stacks. *See id.* at 34 ("Chiricescu literally describes Zavracky as teaching technology 'to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip'" (quoting Ex. 1004, II-232)).

Claim 4 depends from claim 1 and recites "[t]he processor module of claim 1 further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements." Petitioner relies on its analysis of claims 1 and 2, and explains that "the Zavracky-Chiricescu-Akasaka Combination teaches the stacking of microprocessor and FPGA functional elements, but it also teaches that the memory and FPGA functional elements, are 'stacked with and electrically coupled to' each other, readily providing this element." Pet. 35. Petitioner alternatively relies on "other ways" that Zavracky teaches this element, pointing out that the "'third integrated circuit functional element' is not limited to a particular function in this claim." *Id.* As such, Petitioner relies on Zavracky's disclosure of multilayer electrically coupled stacks, including those illustrated in Figures 10, 12, and 13. *Id.* (citing Ex. 1003, Fig. 10, 11:63–65 ("memory may be stacked on top of the multi-layer microprocessor"), Fig. 12, 12:15–28 ("stacked microprocessor and random access memory array [with] buses run vertical through the stack"), Fig. 13, 12:33–35 ("microprocessor [stacked and electrically coupled] with random access memory"); Ex. 1002 ¶¶ 313–326).

Independent claim 5 is a system claim. As Petitioner contends, "[c]laim 5 takes limitations from claim 1 and combines them with a generic processor and memory." Pet. 36. Specifically, claim 5 recites "[a] reconfigurable computer system comprising: a processor; a memory;" and "at least one processor module" that materially recites the same limitations as the "processor module" of claim 1. The processor module of claim 1 reads on the "Zavracky-Chiricescu-Akasaka Combination" as determined above. Other than at most implying some type of electrical connection through the recitation of "a reconfigurable computer system comprising" in the preamble, claim 5 does not specify any electrical communication between the processor, memory, and "processor module."

Petitioner contends that "Zavracky-Chiricescu-Akasaka Combination in further combination with [general knowledge of the POSITA] renders obvious claim 5." Pet. 36. Petitioner explains that the "the Zavracky- Chiricescu-Akasaka Combination teaches the use of numerous microprocessors and numerous memories – any of which can satisfy the additional requirement for one more processor and one more memory in claim 5, and indeed, the teachings of Figure 13 already shows such a reconfigurable computer system." *Id.* "Beyond this," Patent Owner contends that a person of ordinary skill would have known to connect an FPGA of the Zavracky-Chiricescu-Akasaka Combination in a system with memory and a processor as evidenced by admissions in the '951 patent, including prior art Figure 1, which shows a "prior art 'MAP^{TM,} element . . . taught to 'comprise a field programmable gate array "FPGA"

[and] read only memory.'" *Id.* at 36–37 (quoting Ex. 1001, 3:22–24; citing *id.* at Fig. 1). Petitioner points out that admitted prior art Figure 1 is one example that evidences the general knowledge of an artisan of ordinary skill, and "[t]he general knowledge of the POSITA would have other examples of reconfigurable computer systems with a processor, memory, and processor module." *Id.* at 37 (citing Ex. 1002 ¶¶ 267–73, 289; Ex. 1026).[15]

Petitioner points out that admitted prior art Figure 1 shows microprocessor 12 and system memory 16 coupled electrically with the MAP™ (which includes an FPGA). Pet. 37 (annotating Ex. 1001, Fig. 1). Petitioner asserts that it would have been obvious to employ the Zavracky- Chiricescu-Akasaka 3-D stack in a system with processor and memory in order to configure the FPGA using off-chip resources during start-up with a reasonable expectation of success where such systems were well-known. *See id.* at 37–39 (citing Ex. 1003, 12:37; Ex. 1002 ¶¶ 272–73; Ex. 1004, II-234 (describing "during the initiation phase of the application . . . loading configuration data . . . from memory off-chip").

Claim 6 depends from claim 5 and recites "the computer system processor module of claim 5 wherein said third integrated circuit die element comprises a

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[15] In other words, the admitted prior art evidences the knowledge of the ordinary artisan and does not form the "basis" of the rejection. *Cf. Apple Inc. v. Qualcomm Inc.*, 2022 WL 288013, slip op. at *5 (Fed. Cir. Feb. 1, 2022) (holding that that applicant admitted prior art (AAPA) may not form the "basis of a ground in an *inter partes* review because it is not contained in a document that is a prior art patent or prior art printed publication.").

memory." Petitioner points to its analysis of claim 2 to address claim 6. Pet. 39. Petitioner's analysis of claim 2 includes an annotated version of Zavracky's Figure 13, which depicts at least three integrated circuit layers, including memory, a processor, and RAM (random access memory 806). *Id.* at 33.

Claim 8 depends from claim 5 and recites "[t]he computer system of claim 5 further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements." Petitioner relies on its analysis of claim 4 to address claim 8. Pet. 39.

Claim 9 depends from claim 8 and recites "[t]he computer system of claim 8 wherein said third integrated circuit functional element comprises a memory." Petitioner refers to its analysis of claims 1 and 4 to address claim 9. Pet. 40. Petitioner also explains that "Zavracky . . . teaches the POSITA an embodiment where multiple IC functional elements, such as the claimed second and third elements, comprise memory." *Id.* (citing Ex. 1002 ¶¶ 318, 322). Petitioner quotes Zavracky as teaching that "[t]his configuration lends itself well to use in signal processing applications." *Id.* (quoting Ex. 1003, 12:27–28).

Independent claim 10 is materially similar to claim 1 but includes at least a third "integrated circuit functional element" in addition to the at least first and second integrated circuit functional elements, with the three functional elements stacked and electrically coupled (without requiring a number of contact points distributed throughout the surfaces of the functional elements and extending through a thickness thereof

as recited in claim 1). The three functional elements include a programmable array, processor, and memory. Petitioner primarily relies on its showing for claims 1, 4, and 9 to address claim 10. Pet. 40–42. Referring to, and similar to, its analysis of claim 1, Petitioner explains generally that "Zavracky's 3D stack includes multiple IC 'functional elements'," including microprocessor in relation to Figures 12 and 13. *See id.* at 41. Similarly, in its analysis of claim 4, Petitioner states that "Zavracky, for example, describes stacks with at least three layers wherein memory and microprocessor functional elements are stacked and electrically coupled." *Id.* at 35–36 (citing Ex. 1003, Fig. 10, 11:63–65 ("memory may be stacked on top of the multi-layer microprocessor"), Fig. 13 (showing stacked RAM, microprocessor, and PLD/FPGA layers).

Dependent claims 11–15 recite materially the same added limitations addressed above in connection with claims 1, 2, 4, and 10. Petitioner refers to its showing for the latter claims to address claims 11–15. Pet. 43–44.

Independent claim 16 is materially similar to claim 1 but broader, because while, similar to claim 1, it recites "a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element wherein said memory array is functional to accelerate external memory references to the processing element," it does not specifically recite "electrically coupl[ing] by a number of contact points distributed throughout the surfaces of said functional elements," as claim 1 does. Petitioner primarily relies

on its showing for claim 1 to address claim 16. Pet. 44–45.

Independent claim 23 is materially the same as claim 1, with claim 1 reciting a "processor module" in its preamble and a programmable array in its body, and claim 23 reciting a "programmable array" in its preamble and reciting an FPGA in its body, with other differences with respect to coupling that Petitioner's showing for claim 1 addresses. Petitioner primarily relies on its showing for claims 1 and 16 to address claim 23. Pet. 49–50.

Dependent claim 27 depends from independent claim 23 and recites "at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements." Dependent claim 29 depends from claim 27 and recites "wherein said third integrated circuit functional element includes an I/O controller."

To address claim 27, Petitioner relies on its analysis of claim 4. Pet. 50. To address claim 29, Petitioner relies on Zavracky's "'controller' as controlling connections 'to and from the common data bus' and containing 'arbitration logic, hosted in the controller [run] in accordance with [a] bus arbitration protocol.'" *Id.* at 51 (quoting Ex. 1003, 5:54–60). According further to Petitioner, Zavracky's Figure 1 and Figure 13 illustrate the same or a similar controller, and Zavracky discloses a bus controller that arbitrates logic under a bus arbitration protocol to communicate with off-chip resources as "a third IC functional element." *See id.* at 51–52 (citing Ex. 1002 ¶¶ 324–325; Ex. 1003, 6:58–60). Petitioner alternatively relies on another controller in Zavracky

that provides communication protocols between microprocessor and peripheral devices, and contends that "Zavracky teaches that such a programmable I/O controller 'can be formed in any of the layers of a multilayer structure as described elsewhere herein.'" *Id.* at 52 (quoting Ex. 1003, 12:28–38; citing Ex. 1002 ¶¶ 325–326).

We adopt and incorporate Petitioner's showing for claims 1, 2, 4–6, 8–16, 23, 27, and 29, as presented in the Petition and summarized above, as our own. *See* Pet. 7–12, 14–52.

5. *Arguments with Respect to Alleged Obviousness Based on Zavracky, Chiricescu, and Akasaka*

Patent Owner does not argue any of claims 1, 2, 4–6, 8–16, 23, 27, and 29 individually, but groups various claims together in separate arguments, as discussed below. Sections below address claims 17–22, 25, 26, and 27, although Patent Owner groups some of these claims together with claims 1, 2, 4–6, 8–16, 23, 27, and 29 in generic arguments or more specific arguments. We address some of the more generic arguments in this section and other more specific arguments below. *See infra* §§ II.D.6–7; II.E–G.

Patent Owner argues that "[t]he *Zavracky-Chiricescu-Akasaka* combination fails to teach or suggest a 3-D processor module that includes a second integrated die element, separate from a first integrated die element having a programmable array, including a "memory array [that] is functional to accelerate external memory references to said processing element." PO Resp. 19 (listing claims 1, 5, 10, 16, and 23). *See infra* §§ II.4 (analyzing claims 5,

10, 16, and 23, which materially track the limitations of claim 1 based on the issues raised herein). Claims 1, 5, 10, 16, and 23 do not recite die elements, so Patent Owner's argument in that respect is not clear.

In any event, on one hand, Patent Owner admits that "[t]he '951 Patent provides accelerated external memory references due to its technique of stacking a programmable array with a memory die using through-silicon vias (TSVs)." *Id.* On the other hand, Patent Owner contends that "it is not simply stacking of a memory die with a programmable array that accelerates the programmable array's access to memory. . . . [r]ather, as the claims themselves require, it is the structure provided ***within the memory array*** (i.e. the [WCDP] disclosed in the '951 Patent) that is responsible for accelerating the programmable array's accelerated external memory references." PO Resp. 20. The latter argument is a claim construction argument, which we discuss above, and it is unavailing for the reasons noted. *Supra* § II.C (Claim Construction)).

Similarly, as also discussed above (§ II.C), Patent Owner argues that the inventors solved the problem of "loading configuration data through a typical, relatively narrow configuration data port [which] led to unacceptably long reconfiguration times," by "stacking a memory die with a programmable array die" and "interconnecting" them "with a 'wide configuration data port' that employs through-silicon contacts, with the potential for even further acceleration where the memory die is 'tri-ported.'" PO Resp. 20 (citing Ex. 1001, 5:18–25). It is not clear how this argument addresses Petitioner's showing or a claim limitation. As summarized above and further

below, Petitioner shows how the combined teachings of Zavracky, Chiricescu, and Akasaka satisfy the adopted claim construction, namely "a number of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array." *See supra* § II.C.

Patent Owner also argues that "Petitioner's expert admits" in his deposition testimony that "Chiricescu's 'RLB BUS' that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the '951 Patent." *Id.* at 21 (citing Ex. 2012, 80:12–17 ("That memory would be narrower because that's the structure of memory, is you access in DRAM; for example, you wouldn't have thousands of bits wide access to the DRAM in a normal memory structure in this time frame.")). According to Patent Owner, "even though Chiricescu discloses stacking a memory layer with an RLB, its narrow configuration data port still loads configuration data 'in a byte serial fashion and must configure the cells sequentially.'" *Id.* (citing Ex. 1001, 4:55–60; Ex. 2011 ¶ 57).

As discussed further below, Dr. Zavracky does not admit that Chiricescu describes a narrow port between a memory layer and the FPGA/RLB layer. *See* Reply 11 (explaining that Dr. Zavracky's testimony relates to narrow ports for loading data from an *external* (off-chip) memory source to the FPGA module) (citing Ex. 2012, 80:10–22)). There is no credible evidence to support the argument that Chiricescu transfers data from its on-chip memory layer to its RLB ("sea-of-gates") FPGA layer over a

narrow data port or in byte-serial fashion. *See* Ex. 1004, II-232, Fig. 2. Dr. Souri does not cite to any evidence in Chiricescu to support the testimony that "as Dr. Franzon acknowledges, *Chiricescu* discloses only a narrow configuration data port between the RLB and memory layers." Ex. 2011 ¶ 57 (citing Ex. 2012, 80:10–22). Dr. Zavracky credibly testifies that he "did not 'admit' that 'Chiricescu's RLB BUS that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the [challenged patents].'" *See* Ex. 1070 ¶ 68 (testifying "[t]hat is factually an incorrect statement about Chiricescu - Dr. Souri's claim about Chiricescu is not true, and his claim about my testimony is not true"). And in any event, as discussed above and further below, Petitioner relies on the combined teachings of the references as suggesting a large number of vias extending throughout the die areas in contrast to any narrow data port.

Patent Owner also argues that "Petitioner has not demonstrated that its combination of references 'accelerates external memory references to said processing element' over the baseline of the relatively narrow configuration port distinguished in the '951 Patent (and taught in *Chiricescu*)." PO Resp. Patent Owner also argues that "[b]ecause Petitioner fails even to allege that any aspect of *Chiricescu's* 'memory layer' itself is functional to accelerate external memory references, it has not even raised a *prima facie* case of obviousness." *Id.* at 23 (citing Ex. 2011 ¶ 59).

These arguments do not address Petitioner's reliance on multiple vertical vias in the stacked memory chip structure of Zavracky, as modified by the

combined teachings of Chiricescu and Akasaka, to accommodate the memory array operating as a cache or other memory to accelerate the loading of the reconfiguration data. *See* Pet. 17–22, 27–33. Petitioner notes, for example, that "Akasaka teaches that these 'tens of thousands of via holes' permit parallel processing, and that use of the 'via holes in 3-D ICs' shortens the interconnection length between IC die elements so that 'the signal processing speed of the system will be greatly improved.'" *Id.* at 18 (quoting Ex. 1705, 5). Petitioner also states that "Akasaka further explains that 'shorter interconnection delay time and parallel processing' means that the processing of data between layers is accelerated such that '*twice the operating speed is possible* in the best case of 3-D ICs.'" *Id.* (emphasis added) (quoting Ex. 1705, 5). Petitioner also relies on an article by Dr. Franzon and states that "the POSITA in 2001 was also aware of the many advantages of stacking IC die elements, including accelerated processing of data as compared to 2-D devices." *Id.* at 12 (citing Ex. 1020, 2–3; Ex. 1002 ¶¶ 53–57). Petitioner also relies on vias in a "vertical bus" connecting each of Zavracky's layers, including random access memory array layers, to microprocessor layers. *Id.* at 32 (citing Ex. 1003, 11:63–65, 12:15–28, 12:33–35, Figs. 12, 13).

Contrary to Patent Owner's claim construction arguments, apart from numerous vias that the parties agree are part of a WCDP, none of the challenged claims require other aspects of a WCDP and/or buffer cells under our claim construction, and the specification does not describe Figure 5's WCDP (depicted as black box) as part of a memory array. *See supra* § II.C; Ex. 1001, Fig. 5. As Petitioner persuasively argues and as summarized above, the

Petition relies on the combined teachings of Zavracky, Chiricescu, and Akasaka to teach the "functional to accelerate clause." *See* Reply 4–12. As Petitioner also persuasively argues, even if the claims require other structure of a WCDP, according to Patent Owner's expert in IPR2020-01020, IPR2020-01021, and IPR2020-01022, a "**configuration data port** . . . is . . . just a **data port used for configuration** . . . And **data port is just an interface to send data** from one place to another." Reply 9 (emphasis by Petitioner) (quoting Ex. 1075, 163:8–21). "And 'the reason it's a very wide configuration data port is because it has **a lot of connections** through these TSVs between the memory die and the FPGA die.'" *Id.* (quoting Ex. 1075, 157:23–158:3).

In other words, under Petitioner's persuasive showing, even if the challenged claims require some aspects of a WCDP, the combined teachings meet the claims for the reasons noted. Petitioner persuasively shows that the Zavracky-Chiricescu-Akasaka 3-D module uses numerous vias throughout the dies to transfer data *between* the dies—i.e., functional to accelerate all manner of data and signals in parallel (like a WCDP). *See, e.g.*, Pet. 18 (showing that Akasaka teaches that "'tens of thousands of via holes' permit parallel processing" by utilizing the many interconnections; as a result of this parallel processing, "the signal processing speed of the system will be greatly improved"; and due to "shorter interconnection delay time and parallel processing" made possible from the area-wide interconnects, the processing of data between layers is accelerated such that "twice the operating speed is possible in the best case of 3-D ICs" (quoting Ex. 1005, 1705)), 20 (arguing that "it was a predictable advantage and also

suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3-D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity" (citing Ex. 1002 ¶ 233; Ex. 1005, 1705)). Petitioner also shows that "[i]t was well known that 'interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems,' and that '*wide buses are very desirable*' and were made possible by 3-D stacking." *Id.* at 12 (emphasis added) (quoting Ex. 1020, 12).

Patent Owner argues that "in *Akasaka*, the 3-D chip design that uses vertical interconnections is only mentioned for a flip-chip design and a monolithic design, which means it is fabricated as a single piece of silicon with multiple layers." PO Resp. 16. Patent Owner argues that "Akasaka explains that among the expected improvements are the use of '[s]everal thousands or tens of thousands of via holes' in monolithic chips to take advantage of parallel processing." *Id.* at 17 (quoting Ex. 1005, 1705). According to Patent Owner, Akasaka's "flip-chip design is limited . . . in that 'the number of connections are restricted by reliability and bump size constraints.'" *Id.* at 16 (quoting Ex. 1005, 1704).

Contrary to these arguments, Akasaka states that with respect to flip chips, "the number of connections will be greatly increased by this technology." Ex. 1005, 1704. Moreover, Akasaka refers to the flip chip structures in a section titled "3-D IC Structure." *Id.* And contrary to Patent Owner's arguments, Akasaka generally indicates that for all known "3-D structures" at the time, "[s]everal

thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers or vice versa through them." *Id.* at 1705; *see also* Reply 20 n. 6 (showing that 3-D die stacking with numerous chips was well-known known (citing Ex. 1002 ¶¶ 328, 332); *id.* at 21 n. 8 (persuasively showing that Patent Owner "describes Akasaka's teachings inaccurately" (citing 1002 ¶¶ 233–239; Ex. 1070 ¶¶ 59–66); Ex. 1070 ¶¶ 60–61 (disputing Dr. Souri's testimony and stating that Akasaka shows "vertical interconnections between multiple chips and other chip attachment mechanisms," and testifying that "Akasaka does not limit its via fabrication teachings to two layers or a monolithic chip"); Ex. 1002 ¶ 238 (testifying that chip stacking was known and "[t]here were many references teaching stacked dies with thousands of distributed connections, including those discussed in my technology backgrounder above, Section V, and the papers in Section IX"). Akasaka also indicates that even in 1986, about five years before the 2001 date of the invention, artisans of ordinary skill would have mixed flip chip technology and monolithic technology to provide stacked layers: "Mixing of assembly technology with monolithic chip technology can also provide 4 layers or 6 layers from 2-layer or 3-layer stacked monolithic ICs, respectively." Ex. 1005, 1713.

Therefore, Petitioner shows that the numerous via connections between the memory die and FPGA in the modified stack of Zavracky connect to the memory array to render the "memory array functional to accelerate memory references to the processing element," as the challenged claims require. *See, e.g.*, Pet. 20–21 (showing that Akasaka's numerous connections would have motivated a POSITA to

replicate common data memory, and "increase bandwidth and processing speed through better parallelism and increased connectivity"); 32 (relying on Zavracky's "random access memory array [with] buses run vertical through the stack" implemented as a cache memory according to Chiricescu's teachings in order to accelerate access to memory references and reconfigure the FPGA (quoting Ex. 1004, 12:15–28; citing *id.* at 11:63–65, Figs. 12, 13; Ex. 1004, II-232)).

As indicated above, Petitioner also persuasively shows that Patent Owner "misrepresents Dr. Franzon's testimony" regarding an alleged narrow port in Chiricescu. *See* Reply 11. As Petitioner persuasively argues, "Dr. Franzon's cited testimony: (1) has nothing to do with Chiricescu; (2) was given in response to a question about Trimberger; and (3) was discussing the connection to "an **off-chip** memory." *Id.* (citing Ex. 2012, 80:10–22).

Dr. Franzon's cited deposition testimony supports Petitioner. Dr. Franzon's cited deposition testimony refers to Trimberger in the context of "off-chip memory that loads in through the data port," and Dr. Franzon testifies "a POSITA would interpret figure 5 [of the '951 patent] as [including an undepicted] similar narrow structure on the left of the very wide configuration data port" to load data from an external source. *See* Ex. 2012, 80:3–22. In other words, Dr. Franzon's testimony does not describe Chiricescu's stacked memory layer as using a *narrow* port to transfer reconfiguration data to the RLB (with FPGA gates) layer from this "on- chip" memory within the 3-D stack. *See* Ex. 1004, Fig. 2; *supra* § II.D.2; Ex. 1070 ¶ 68 (refuting Dr. Souri's testimony and

characterization with respect to Chiricescu and Dr. Franzon's testimony about Chiricescu).

As Petitioner also argues, Patent Owner's "'narrow data port' arguments are contrary to Chiricescu's teachings" and do not address the combined teachings of Chiricescu, Zavracky, and Akasaka. Reply 11 (citing PO Resp. 20–21). Petitioner notes that Zavracky describes "interconnects as being '*placed anywhere on the chip*' without restriction." *Id.* (emphasis added) (quoting Ex. 1004, 232). In addition, Petitioner notes that Chiricescu "discloses 'three separate layers with metal interconnects [including a "memory layer"] between them.'" *Id.* (quoting Ex. 1004, 232) (addition by Petitioner) (emphasis omitted). Vias running everywhere throughout the different stacked layers or dies, as Zavracky, Chiricescu, and Akasaka individually and collectively teach, distinguish over any alleged narrow port, and Petitioner provides well-known reasons for employing numerous vias of wide data ports, such as allowing for increased bandwidth and parallelism. *See* Pet. 12, 18, 20 (discussed and quoted above); Ex. 1001, 5:16–21 (describing "through-die array contacts 70 . . . routed up and down the stack in three dimensions" as "not known to be possible with any other currently available stacking techniques *since they all require the stacking contacts to be located on the periphery of the die*," so that by placing contacts throughout, "*cells that may be accessed within a specified time period is increased*") (emphasis added).

With respect to all challenged claims, Patent Owner also argues that "Petitioner and Dr. Franzon fail to explain how a POSITA would have integrated Akasaka's thousands of distributed contact points

with Zavracky- Chiricescu's design to achieve the claimed 3-D processor modules and would have had a reasonable expectation of success in doing so." PO Resp. 38 (citing Ex. 2011 ¶ 78). According to Patent Owner, "Petitioner and Dr. Franzon concede that *Zavracky* and *Chiricescu* both disclose only a small number of interconnect paths (e.g., the address and data buses) that provide for vertical communications between functional blocks (such as memory elements, logic unit, etc.) of the multi-layer microprocessor." *Id.* (citing Ex. 1003, 11:62–12:39; Ex. 1004, 1–2). According further to Patent Owner, "Dr. Franzon's analysis, like Petitioner's analysis, seems to say no more than that a POSITA would have understood that the references ***could be*** combined." *Id.* at 40 (citing Ex. 1002 ¶ 239). Patent Owner also asserts that "[a]t the time of the invention, a POSITA was aware of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ("HDL") algorithms, which must be considered." *Id.* at 41 (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89).

Patent Owner's arguments are unavailing. As discussed above, Petitioner persuasively relies on the knowledge of the artisan of ordinary skill and the combined teachings of Zavracky, Chiricescu, and Akasaka supported by specific reasons and rational underpinning to show how the combination teaches or suggests increasing the number of contact points or via holes for electrically coupling FPGA, memory, and processors together. Petitioner also shows the "why"––to allow for parallel data transfers, speed increases, larger bandwidth, etc., all with a reasonable expectation of success.

As indicated above, Zavracky already specifically describes connecting several bus lines (depicting 4 in Fig. 13) from the FPGA/PLD to other circuits, including memory and a processor. *See* Pet. 23–24. Patent Owner contends that "Zavracky proposes using these vertical connections 'for the same reasons any lines otherwise restricted to a single layer are used.'" PO Resp. 10 (quoting Ex.1003, 6:48–49). This argument supports Petitioner, because it shows that an artisan of ordinary skill easily would and could have re-routed connections of known circuitry using vias. Petitioner shows a number of other stacked dies or layers with multiple via connections, including Akasaka (Ex. 1005, Fig. 4), Franzon (Ex. 1020, Fig. 4), Koyanagi (Ex. 1021, Fig. 1(a)), and Alexander (Ex. 1028, Fig. 2(g). *See* Pet. 31. As discussed further below, Trimberger (Ex. 1006) shows parallel loading by "*flash reconfiguring* all [100,000] bits in logic and interconnect array [i.e., an FPGA] . . . simultaneously from one memory plane." *See infra* § II.E.1 (quoting Ex. 1006, 22).[16]

Patent Owner concedes Zavracky and Chiricescu each show how to connect "memory, logic, etc." using "address and data buses," albeit on what Patent Owner describes as "only a small number of interconnect paths." PO Resp. 38 ("*Zavracky* and *Chiricescu* both disclose only a small number of interconnect paths (e.g., the address and data buses) that provide for vertical communications between functional blocks (such as memory elements, logic

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[16] Petitioner employs Trimberger to address challenged claim 25 as discussed further below (§ II.E), but it is further evidence of a reasonable expectation of success as it relates to connecting several thousands of bit lines in parallel.

unit, etc.) of the multi-layer microprocessor."). But Patent Owner also agrees that the number of interconnects is not critical to the claimed invention. *See supra* § II.C (discussing Oral Hearing arguments); Tr. 49:1–9 (answering "yes, . . . if you have a very, . . . small FPGA, the number of bits can be . . . relatively smaller, but what's critical is not the number of bits and . . . . [i]t's not necessarily the number of bits that's in the configuration data port, but how they're arranged"). In any event, Petitioner shows that a large number of vias would have been obvious in view of the combined teachings, to enhance speed, allow parallel processing and data transfer, minimize latency, and maximize bandwidth, as noted throughout this Final Written Decision.

Alleging a lack of a reasonable expectation of success, Patent Owner acknowledges that "[a]t the time of the invention, *a POSITA was aware* of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ('HDL') algorithms." PO Resp. 41 (emphasis added) (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89). Here, the challenged claims are broad and do not specify a minimal number of interconnections, FPGA size, or chip size that would even raise TSV congestion or other issues. The '951 patent says nothing about interconnection issues or congestion. Even if such issues were a consideration and relevant to a reasonable expectation of success given the breadth of the challenged claims, as Petitioner persuasively argues, "[t]he supposed 'TSV interconnection issues' that [Patent Owner] cursorily identifies were at most normal engineering issues, not problems preventing a combination." Reply 20 (citing

Ex. 1070 ¶¶ 13–28 (Dr. Franzon addressing Dr. Souri's testimony as to the purported TSV issues)).

> For example, as Dr. Franzon credibly testifies,
>
> > even if routing congestion or TSV placement were an issue, Kim gives several solutions that would have been known to POSITA, such as to change the TSV "coarseness" or to "increase the chip area to address the placement and routing congestion caused by TSV insertion." [Ex. 2014 (Kim), 85]. But again, the ['951] patent[] and claims are silent on any of these issues; Kim is at worst irrelevant, and at best would have actually encouraged the combination.

Ex. 1070 ¶ 26. With respect to alleged HDL (hardware description language) issues, Dr. Franzon also credibly testifies that

> Alexander (Ex. 1009) has a whole section titled "Placement and Routing in 3D" (Ex. 1009, p. 256). Alexander names then- existing CAD tools that performed these functions, including DAGmap and Mondrian. Designing distributed 3D interconnects was a routine engineering problem by the time of the Huppenthal Patents, and not an impediment to reasonable expectation of success in making the Zavracky, Chiricescu, Akasaka combination.

Ex. 1070 ¶ 27.

Petitioner provides other evidence that at the time of the invention, an artisan of ordinary skill would have had a reasonable expectation of success in combining the references to arrive at multiple vias connecting circuits (including memory arrays) on stacked chips and to allow for parallel processing or

data transfers. *See, e.g.*, Pet. 8–13 (discussing known wafer processing technology by artisans of ordinary skill supported by evidence (citing Ex. 1002 ¶¶ 47–51, 262–266; Ex. 1001, 2:29–35; 5:13–18; Ex. 1009, Fig. 2; Ex. 1020, 5, 9–12, Fig. 4; Ex. 1021, 17, Fig. 1(a); Ex. 1022; Ex. 1023, Fig. 4(b); Ex. 1025, code (57), 1:59–65, 2:11–13, Fig. 1; Ex. 1027, code (57); Ex. 1030, 94; Ex. 1031, 70)), 28–29 (pointing to Zavracky's memory as an example vertical integrated circuit on stacked dies connected by via connections including vertical buses "placed anywhere on the die" and providing evidence that "each of the programmable array, microprocessor, and memory are pairwise stacked with and electrically coupled with each other" (citing Ex. 1003, 2:7–8, 2:18–22, 2:27–35, 6:43–7:9, 10:8–21, 11:63–12:2, 12:13–39, 14:51–63, Fig. 13), 25–26 (further relying on Akasaka as teaching thousands of vias to connect upper and lower circuit layers (citing Ex. 1005, 1705, 1707; Ex. 1002 ¶¶ 327–332)). Furthermore, the '951 patent describes "recently available wafer processing techniques" including those developed by "Tru-Si Technologies," indicating, for purposes of institution, that artisans of ordinary skill would have been aware of any such wafer processing techniques for forming vias at the time of the invention. *See* Ex. 1001, 2:19–40. Therefore, Petitioner persuasively shows ample evidence of a reasonable expectation of success.

In addition, as noted above, Patent Owner argued during the Oral Hearing that the number of contacts is not important, depending on the size of the FPGA, provided that the contacts allow for parallel processing. *See supra* § II.C (discussing Tr. 49:1–9 (Patent Owner arguing that the number of vias "could be as small as 32 bits . . . if you have a small FPGA,

. . . . [and] [i]f you want to update something in parallel, you could update 32-bit with 32 bits," further stating that "if you have a very . . . small FPGA, the number of bits can be . . . relatively smaller, but what's critical is not the number of bits"). The challenged claims at issue here do not specify an FPGA size.

In any event, as summarized above, Petitioner provides persuasive motivation with a reasonable expectation of success to explain why a person of ordinary skill would have increased the number of vias using known techniques, relying on teachings that providing multiple vias in stacked chips using conventional via and metallization processing allowed for faster processing speeds and reconfiguration times, shorter latency, higher bandwidth, and parallel processing, with a known desire for wide buses. *See* Pet. 7–12, 18–22; Ex. 1002 ¶¶ 53–57; 212–239. Dr. Franzon also shows that the combined teachings of Zavracky and Chiricescu suggest "processing tasks . . . [in] co-stacked microprocessors and memories as good applications for 3-D stacked chips that required parallel computation." Ex. 1002 ¶ 229.

As Petitioner also persuasively notes, Zavracky does not limit the number of connections, contrary to Patent Owner's arguments. For example, Petitioner quotes Zavracky as describing "**inter-layer connections** [that] provide for vertical communication. . . . [and] [s]uch connections can be placed **anywhere on the die** and therefore are not limited to placement on the outer periphery." Reply 4–5 (emphasis by Petitioner) (quoting Ex. 1003, 6:43–47) (emphasis by Petitioner). Petitioner quotes Zavracky as teaching "buses run vertically through the stack by

the use of inter-layer connectors" in describing Figures 12 and 13. *Id.* (quoting Ex. 1003, 12:24– 26). Petitioner persuasively explains that "Zavracky visually shows a number of vertical contacts that traverse the memory die in the internal periphery of the die and provide contacts on the surface of the memory die, just as the Board's construction requires." *Id.* at 5–6 (annotating Ex. 1003, Figs. 12, 13).

Petitioner also persuasively relies on Zavracky's teaching that "this approach **accelerates** communication between the dies in the chip by way of "**smaller delays** and **higher speed** circuit performance." Reply 6 (emphasis by Petitioner) (quoting Ex. 1003, 3:4–14). Petitioner persuasively notes that Chiricescu describes Zavracky's teachings as "allow[ing] us" to build stacked circuit layers on a chip with "vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip." *See id.* (quoting Ex. 1004, 232). Petitioner also persuasively argues that Chiricescu teaches the recited "functional to accelerate" clauses, with "significantly **improved[d FPGA] reconfiguration time**" through its "interconnected layers, including a memory layer configured as a cache for fast access to 'configuration data . . . from memory off-chip.'" *Id.* at 6 (quoting Ex. 1004, 232) (emphasis by Petitioner). Other than disclosing an 8-bit configuration port as prior art with respect to Figure 3, the '951 patent does not specify how many via interconnections the claimed "accelerate" functionality requires. *See id.* at 2:56–3:2 (describing stacking an FPGA with a "memory die" "for the purpose of accelerating FPGA reconfiguration" and "for the purpose of accelerating external memory references" and stacking "a

microprocessor, memory and FPGA . . . for the purpose of accelerating the sharing of data"), 5:20–21 (describing cache memory purpose of serving "its traditional role of fast access memory").

Patent Owner restricts Chiricescu teachings as suggesting only "the use of 'on-chip' memory to mitigate the time it takes to transfer configuration data from 'off-chip,' rather than making any use of Zavracky's die-area vertical interconnections to transfer configuration data from the 'on- chip' memory into the FPGA." *See* PO Resp. 29 (citing Ex. 1004, 1, 3). Patent Owner also argues that "[n]either *Zavracky* nor *Chiricescu* even contemplate using die-area inter-layer vertical interconnections to move data between a programmable array and a memory, such as is recited in Claims 1, 5, 10, 16, 18, and 23." *Id.* at 29 (citing Ex. 2011 ¶ 66). The record does not support this line of argument. As discussed above, Zavracky's Figure 13 shows that Zavracky contemplates moving data on vertical buses between RAM memory 808 (and RAM memory on processor layer 806) and programmable array 802 (Ex. 1003, 12:29–39), and Chiricescu's Figure 2 shows that Chiricescu contemplates moving data on "vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip" (based on Chiricescu's characterization of Zavracky) between memory layer and the "sea of gates FPGA" RLB layer (Ex. 1004, II-232); *see also* Ex. 1004, II-232 § 1 ("Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.").

Also, Petitioner shows persuasively that an artisan of ordinary skill would have recognized that

speed improvement emanates largely from shorter interconnection distances and/or parallel processing using a large number of vias (as compared to long metal connections running on the same plane). *See* Reply 6 (arguing Zavracky's "approach **accelerates** communication between the dies in the chip by way of '**smaller delays** and **higher speed** circuit performance'" (emphasis by Petitioner (quoting Ex. 1003, 3:4–14)), and arguing that "Zavracky's short interior 'inter-layer connectors' to stacked 'random access memory . . . results in **reduced** memory access **time**, **increasing the speed** of the entire system.' (emphasis by Petitioner (quoting 11:63–12:2)).

Patent Owner's observations support Petitioner. For example, asserting that "[t]he '951 Patent provides accelerated external memory references due to its technique of stacking a programmable array with a memory die using through silicon vias (TSVs)," Patent Owner quotes the '951 patent as providing "increased" "bandwidth" and providing the "traditional role of fast access memory." *See* PO Resp. 19–20 (quoting Ex. 1001, 5:18–28).

Patent Owner also argues that "[b]ecause Petitioner does not allege that any 'external memory references' occur in *Chiricescu* (let alone that such references are accelerated), Petitioner cannot have met its burden to establish that Claims 1, 5, 10, 16, and 23 and their dependents are obvious." PO Resp. 23. According to Patent Owner, "Petitioner misinterprets the term 'external memory references,' suggesting that this term too can be satisfied simply by storing a certain type of data in Chiricescu's memory." *Id.* (citing Pet. 32–33; Ex. 1002 ¶ 307). Patent Owner also argues that "memory references

are not data, but are instructions directed to a particular place memory address [sic] in memory." *Id.* (citing Ex. 2011 ¶ 60; Ex. 2015, 181; Ex. 2012, 49:11–50:1).

These arguments are unavailing. Dr. Souri's cited declaration testimony does not tie his opinion that "[a] skilled artisan understands that memory references are not data" to the limitations recited in claim 1, 5, 10, 16, and 23 as viewed in light of the '951 patent specification. *See* Ex. 2011 ¶ 60. In addition to citing the Dr. Franzon's deposition testimony, which does not support Dr. Souri as indicated above, Dr. Souri cites "Ex. 2015 at 181." This particular extrinsic evidence, which includes a single page out of what appears to be a text book, is not helpful because it does not have anything to do with accelerating memory references, and it describes types of "operands," which are not at issue in the '951 patent. *See* Ex. 2015, 181 ("The third type of operand is a memory reference."). In other words, Dr. Souri's testimony is conclusory as it does not address how this extrinsic evidence relates to the recited "functional to accelerate external memory references" clause as recited in the challenged claims and in the context of the cache memory or reconfiguration scheme as set forth in the '951 patent specification. *See* Ex. 2011 ¶ 60 (citing Ex. 2015, 181). Patent Owner and Dr. Souri also do not explain clearly how the cited deposition testimony of Dr. Franzon supports Patent Owner. *See* PO Resp. 23 (citing Ex. 2012, 49:11–50:1; Ex. 2011 ¶ 60); Ex. 2012, 49:11–50:1 (generally testifying that "Chiricescu's FPGA processing element" is "agnostic" as "to what actually is stored in it").

Petitioner persuasively shows that caching external memory references in a stacked cache memory satisfies the "functional to accelerate" limitations relative to loading them from off-chip (outside of the stack), because of "caching" *and* "the use of short electrical paths, or significantly increased number of connections," including "Akasaka's area-wide distributed interconnects." *See* Reply 8 (citing Pet. 13–31, 44–47); *see also id.* at 12 (discussing hitting the cache with external memory references (citing Ex. 1002 ¶¶ 215–216; Ex. 2012, 42:9:14, 48:6–50:1)).

Petitioner also persuasively explains that even under Patent Owner's narrow interpretation of "external memory references" as related to memory addresses, Chiricescu teaches that interpretation because the memory address references will "hit" the cache. *See* Reply 11–12 (citing Ex. 1002 ¶¶ 215–216). Supporting Petitioner, Dr. Franzon persuasively testifies at the cited paragraphs of his declaration as follows:

> 215. . . . The POSITA would recognize that what Chiricescu is teaching is to use that memory as a "cache" . . . . By doing so, the FPGA's external memory references . . . will be accelerated because [they] will "hit" in the "cache" and be returned from the on-chip memory without having to go off-chip.
>
> 216. Chiricescu is thus teaching to the POSITA to accelerate memory lookups that are directed to the external chip by sending them instead to the on-chip memory, perhaps keeping a relevant set of data to the application. This is what Chiricescu means when it says that "a management scheme

> similar to one used to manage cache memory can be used to administer the configuration data."

Ex. 1002 ¶¶ 215–216; Reply 12 (quoting part of the same two paragraphs).

As Petitioner also persuasively argues, the '951 patent does not limit "external memory references" in particular, but it does refer to cache memory and enhancing reconfiguration speed with such memory. *See* Reply 12 (citing Ex. 1001, 2:11, 2:25, 4:31, 4:57–58); Ex. 1001, 4:31–36 (referring to "cache memory 66" as serving its "traditional role of fast access memory," and also including accessing by "both the microprocessor 64 and FPGA 68 with equal speed," in the context of "reconfigurable computing systems").

Patent Owner also argues that "[b]ecause the claims require a '***memory array*** is functional to accelerate external memory references to said processing element,' Petitioner's focus on the type of data stored in the array misses the mark." PO Resp. 23 (citing Ex. 2012, 43:13–44:3, 49:20–50:1). Contrary to this argument, as discussed above, Petitioner relies on a cache memory array as combined in a 3-D stack with short via connections, not the type of data. As discussed throughout this Final Written Decision, the Petition persuasively relies on such short and numerous distributed vias as structure for the "functional to accelerate" clauses, because such structure provides shorter path delays and allows for increased bandwidth and parallel data transfer from a memory in the stack, including cache memory. *See supra* § II.D.3 (Akasaka's parallel processing and multiple via teachings); Pet. 7–12, 18–22; Ex. 1002 ¶¶ 53–57, 212–239. Essentially, the cache memory relied upon by Petitioner carries all of these

advantages because it is within Zavracky's modified 3-D stack with the FPGA and microprocessor.[17]

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[17] Throughout its briefing, Patent Owner limits all "on-chip" advantages to a *single die* and confuses issues by arguing that even chips in the same stack are "off-chip" relative to each other, such that all "off-chip" vias are part of a "narrow" data port—even with thousands of vias connecting chips in the same stack as proposed by Petitioner. On the other hand, Petitioner, like Zavracky, generally refers to "off-chip resources" to refer to a resource *outside* of a *chip stack*. *See*, *e.g.*, Pet. 51 ("The data bus is used to 'provide communication between logic units or between a logic unit and off-chip resources.'" (quoting Ex. 1003, 5:49–52)); Ex. 1003, 5:53–54 ("Paths which connect off-chip are routed to bonding pads 226 [Fig. 1], which are bonded to the chip carrier pins."); Ex. 1070 ¶ 44 (Dr. Franzon noting that "Dr. Souri apparently means 'chip' here as limited to a single die."). Patent Owner exploits this difference of terminology usage to confound issues, characterizing, for example, Dr. Franzon's testimony as follows: "Dr. Franzon's testi[fies] that '*off-chip* access [*e.g.*, *off-chip* memory separate from the FPGA die] can't be, for example, 100,000 bits wide." Sur-reply 9 (emphasis added) (second bracketed information by Patent Owner). As another example, Patent Owner argues that Petitioner "rel[ies] on Dr. Franzon's discussion that thousands of interconnections for *off-chip* access of a 3D stacked structure is not feasible." *Id.* (emphasis added (citing Reply 18)). This conflation is the opposite of Dr. Franzon's testimony and Petitioner's showing. The thrust of Dr. Franzon's testimony and Petitioner's showing is that numerous stacked via connections in a stack of chips (dies) or layers of a single chip are better (faster, shorter, less congested, etc.) than connections running on the same plane. *See, e.g.*, Reply 17–18 (characterizing Dr. Franzon's testimony as "noting the routine use of on-chip area-wide connections in 3D stacks, including his prior work." (citing Ex. 1020; Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68)); Ex. 1070 ¶ 44 ("But a POSITA would have recognized that [a] 3D chip that consists of multiple dies would do a better job than the 2D chip and provid[e] fast large connectivity. . . . The point here is that a shorter vertical interconnect allows for a shorter 'longest path' and a faster chip. This was commonly understood in the

In the Sur-reply, Patent Owner argues that "[t]he entire point of *Chiricescu* is that it achieves accelerated FPGA configuration by storing configuration data 'on-chip' so that it does not need to load configuration data from off-chip." Sur-reply 5. Patent Owner also argues that "all off- chip connections are carried out through a typical narrow configuration data port, that suffers the same problems as the prior art distinguished in the '951 Patent." *Id.* Patent Owner then argues that "moving *Chiricescu's* cache memory off-chip (i.e., into *Zavracky's* 3-D stacked memory die) eliminates the benefit gained from moving the memory on-chip, [so] a POSITA would not have contradicted *Chiricescu's* fundamental teachings to arrive at Petitioner's proposed combination." *Id.* at 5–6.

These arguments mischaracterize Petitioner's showing and confuse the issues. *See supra* note 17. Patent Owner essentially conflates narrow ports having large signal delays over long electrical planar paths with "all off-chip connections" as applying to Zavracky's 3-D stack by referring to each separate chip in Zavracky's modified 3-D stack as "off-chip" and ignoring the central fact that each chip in Zavracky directly connects to the other chips in the 3-D stack by numerous short vias. There is no support for this line of argument. Moreover, "Dr Franzon not[ed] the routine use of on-chip area-wide connections in 3D stacks, including his prior work." Reply 17–18 (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65; Ex. 1020; *see also* Ex. 1004, Fig. 2, II-232 § 1 (describing "on chip random access memory . . . provided to store

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other art as well. . . . [such as] Akasaka's . . . 3-D 'high speed performance'" (citing Ex. 1005, 1705)).

configuration memory"—i.e., the memory layer of Figure 2). Patent Owner agrees that Chiricescu discloses "on-chip cache memory" as a separate layer of an FPGA chip, further suggesting providing a separate layer in Zavracky's modified stack of layers. *See* Sur-reply 5.

Nevertheless, Patent Owner contends that "the movement of *Chiricescu's* on-chip cache memory to *Zavracky's* off-chip memory would throttle" speed gains. Sur-reply 5. For the reasons explained above, this line of argument confuses issues and mischaracterizes Petitioner's showing. *See supra* note 17. Chiricescu's teachings bolster Zavracky's FPGA teachings, and Petitioner shows that in this context, Zavracky describes a memory layer, microprocessor layer, and FPGA layer in a 3-D stack with each layer connected by numerous short vias to increase speed and provide other advantages. *See, e.g.*, Pet. 14–15, 23–33. Patent Owner's attempt to conflate all "off-chip" narrow port disadvantages to Zavracky's modified stack of chips by calling chips in that stack "off-chip" is unsupported. As Petitioner persuasively shows throughout its briefing, Zavracky's stack of chips, connected by numerous vias, and bolstered by Akasaka's numerous via and Chiricescu's FPGA teachings, operates just like Chiricescu's "on- chip" circuit layers in a single chip connected by numerous vias in terms of speed and acceleration. *See* Reply 6 ("Zavracky's short interior 'inter-layer connectors' to stacked 'random access memory . . . results in **reduced** memory access **time**, **increasing the speed** of the entire system,'" and "Chiricescu also teaches the **acceleration** advantages and 'significantly **improve[d FPGA] reconfiguration time'** achieved by its interconnected layers, including

a memory layer configured as a cache for fast access to 'configuration data . . . from memory off-chip.'" (quoting Ex. 1003, 11:63– 12:2; Ex. 1004, 23[4])), 7 (noting Akasaka's "**acceleration** advantages" based on "teaching, e.g., that '[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing' and that 'shortening of interconnections and signal transfer through vertical via holes in the 3-D configuration provides advantages for the design of large-scale systems.'" (quoting Ex. 1005, 1705)). In other words, as Petitioner shows, in addition to "stacking techniques," "[t]he Zavracky-Chiricescu-Akasaka Combination also discloses the other ways that the '951 patent even arguably implies increases speed—i.e., through caching, the use of short electrical paths, or significantly increased number of connections." *Id.* at 8 (citing Pet. 14–22).

Patent Owner similarly contends that "Dr. Franzon admitted that a wide configuration data port that accelerates a programmable array's external memory references to a stacked memory die as compared with the slow narrow bus disclosed in Chiricescu was not obvious at the time of the invention." PO Resp. 33 (citing Ex. 1012, 71:19–72:1). Based on this contention, Patent Owner also argues that "the wide configuration data port of the '951 Patent provides precisely the answer to what Dr. Franzon admits was practically impossible at the time of the invention." *Id.* at 33–34 (citing Ex. 1012, 71:19–72:1, 80:3–22; Ex. 1011 ¶ 72). Patent Owner adds that this "skepticism of Petitioner's own expert demonstrates that the challenged claims are patentable." *Id.* at 34 (citing Ex. 1011¶ 73). Contrary to this line of argument, similar to the discussion above, Dr. Franzon does not admit that a wide

configuration data port was not obvious, and does not admit that Chiricescu discloses a narrow data bus for transferring data between its stacked layers. *See* Ex. 1012, 71:19–72:1, 80:3–22; *supra* note 17. Rather, at the cited deposition testimony, Dr. Franzon testifies that "*off-chip* [i.e., external] access can't be, for example, 100,000 bits wide." Ex. 1012, 71:21–23. Here, in context, Dr. Franzon states that "you can't have that number of IO. . . . in [the] *case of Trimberger and the '226 patent* [which is related to the '951 patent, *see* IPR2020-01571] *memory going form the external to the module*." *Id.* at 71:23–72:1 (emphasis added). Here again, Patent Owner conflates a narrow data port from a data source "external to the module" (i.e., external to the claimed 3-D stack) with a wide data port from a memory *within the stack* to other chips *in that stack*.

Patent Owner argues that "*Chiricescu* says . . . [that] '[t]he elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application.'" Sur-reply 4–5 (quoting Ex. 1004, 234). Based on this "off- chip" characterization, Patent Owner argues that "Petitioner concocts its hypothetical structure based on its demonstrably false claim that *Chiricescu's* improved FPGA reconfiguration time 'is achieved by its interconnected layers, including a memory layer configured as a cache for fast access to "configuration data . . . from memory off-chip."'" *Id.* at 4 (quoting Reply 6; last internal quote quoting Ex. 1004, II-234). Patent Owner contends that "*Chiricescu* says just the opposite." *Id.* at 5 (citing Ex. 1004, 234).

Again, contrary to this line of argument, Petitioner's showing is opposite to how Patent Owner characterizes it. In other words, Petitioner argues that Chiricescu improves FPGA reconfiguration time because Chiricescu's cache pre-stores and holds configuration data on-chip that it obtains from an external source (i.e., off-chip memory)—so that the FPGA need not access that external (off-chip memory) source to load the FPGA through a "typical narrow configuration data port" (Sur-reply 5) during FPGA reconfiguration. *See* Reply 6; Ex. 1004, II-234 ("The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application."); *see also supra* n.17. In other words, it is because of the numerous short vias within Chiricescu's layered chip that it reconfigures the FPGA/RLB layer from the stacked memory layer more quickly as compared to reconfiguring it through long data lines from an external source. *See* Ex. 1004, II-232, II-234, Fig. 2.

Petitioner also persuasively addresses Patent Owner's argument that the claims require acceleration over a "baseline" and other related arguments. *See* PO Resp. 20–22; Reply 11–12 (persuasively arguing that the combined teachings contribute to acceleration, the combination does not include a "narrow port," and "Dr. Franzon testified in both his declaration and deposition that the Zavracky-Chiricescu-Akasaka combination provides acceleration compared to the baseline of other prior art with different structural characteristics." (citing Ex. Ex. 1002 ¶¶ 212, 215–17, 304–05; Ex. 2012, 28:9–21, 29:15–33:15)); *see also supra* §§ II.C (claim construction in relation to prior art Figure 3's 8-bit

narrow port—i.e., one type of baseline). Zavracky by itself, for example, indicates that 32 bit microprocessors were routine in 1993, years before the effective date of the invention, indicating that Zavracky's microprocessor buses at least handled 32 bits in parallel. *See* Ex. 1003, 1:6–8 (continuity date of 1993), 31–40 (discussing prior art microprocessors). As noted above, Patent Owner indicated during the Oral Hearing that the challenged claims embrace devices transfer data over a port that "could be as small as 32 bits . . . if you have a small FPGA, right? If you want to update something in parallel, you could update 32-bit with 32 bits?" Tr. 49:1–9; *supra* § II.C (claim construction)

Patent Owner also argues that "major modifications would need to be made to the combination of *Zavracky* and *Chiricescu* in order to configure a stacked module to meet the acceleration limitations of Independent Claims 1, 5, 10, 16, and 23." PO Resp. 32. Patent Owner explains that this major modification requires a "wide configuration data port (or other similar structure) between the memory and the FPGA." *Id.* Patent Owner also argues that such a modification would "alter *Chiricescu's* principle operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB Bus and its 'routing layer,' which *Chiricescu* declares '***is of critical importance*** since it is used for the implementation of the interconnection of the non-neighboring RLBs.'" *Id.* (quoting Ex. 1004, 2) (emphasis by Patent Owner).

Here, Patent Owner concedes that "the '951 Patent discloses a memory array that achieves the claimed acceleration (*i.e.*, utilizing a *portion of the*

wide configuration data port), which significantly reduces the amount of time it takes to move data from a memory die into a programmable array." PO Resp. 33 (emphasis added). Patent Owner does not describe what "portion" of the wide configuration data (which Figure 5 of the '951 patent depicts as a black box) the claimed "functional to accelerate" limitations require.

With respect to Chiricescu's principle of operation, as Petitioner also persuasively argues, no "'modifications' are required to Chiricescu at all because the Petition's combination involves 'fold[ing] in Chiricescu's teachings (including using stacked memory to reconfigure[] the FPGA) with Zavracky's 3D stacks." Reply 17 (quoting Pet. 19). Even if employing Chiricescu's FPGA structure also suggests implementing its routing layer on a separate layer, contrary to Patent Owner's arguments, Chiricescu does not describe its routing layer as a narrow port. *See id.* (noting that Dr. Franzon did not admit Chiricescu includes a narrow port and citing Dr. Franzon's testimony that on-chip area-wide connections in 3-D stacks were well- known (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68)). Also, Chiricescu's Figure 2 depicts connections between the memory layer, routing layer, and RLB layer (a "sea-of-gates FGPA structure") with connections that are distinct from the RLB bus. Ex. 1004, II-232 § 2.1, Fig. 2. Chiricescu notes that "routing congestion will also be improved by the separation of layers," further suggesting that the routing layer is not part of a narrow port and suggesting stacking of separate layers in Zavracky's stack. *Id.* at II-232.

As Petitioner persuasively argues, "Chiricescu describes 'vertical metal interconnections (i.e.,

interlayer vias),' and '**three separate layers with metal interconnects between them**.'" Reply 15 (citing Ex. 1004, II- 232). Chiricescu's "express 'architecture is based on' technology developed by Zavracky at Northeastern University." *Id.* (quoting Ex. 1004, 232). And Chiricescu states that Zavracky's architecture provides "3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) *placed anywhere* on the chip." *Id.* at II-232 (emphasis added). Therefore, contrary to Patent Owner's arguments, Chiricescu's principle of operation does not require a narrow port. *See also* Reply 15 ("The combination involves 'fold[ing] in Chiricescu's teachings (including using stacked memory to reconfigure the FPGA) with Zavracky's 3D stacks.'" (citing Pet. 19)). Increasing via connections based further on Akasaka's teachings would have been obvious by facilitating more connections between well-known available circuits such as memory, FPGA, and processors. *See, e.g.*, Reply 19 ("Zavracky and Chiricescu envision connections 'anywhere on the die.'" (citing Pet. 20–22; Ex. 1002 ¶¶ 41–51, 237–238)); Pet. 22 ("Akasaka's distributed contact points would have been the logical extension to Zavracky and Chiricescu's teaching of connections anywhere, especially in view of the POSITA's background knowledge." (citing Ex. 1002 ¶ 239)).

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 1, 2, 4–6, 8–16, 23, 27, and 29 would have been obvious.

6. *Claims 17 and 24*

As determined above (§ II.D.5), independent claims 16 and 23 are materially the same as claim 1, and Petitioner largely relies on its showing for claim 1 to address those independent claims. Pet. 44–45, 49–50. Claims 17 and 24 respectively depend from independent claims 16 and 23 and recite "wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as said processing element." Petitioner relies on its showing in claim 1, including Chiricescu's disclosure about accelerating FPGA reconfiguration using a memory array. *See* Pet. 45, 49–50.

Further regarding claims 16 and 23, as discussed above in connection with claim 1, Zavracky discloses a random access memory layer, or memory array, with buses running through the vertical stack that contains a microprocessor, FPGA, and memory. *See* Pet. 32 (citing Ex. 1003, Figs. 10, 13, 11:63–65, 12:33–35). Chiricescu describes using a random access memory layer as a cache memory to reconfigure the FPGA as a processing element. *Id.* (citing Ex. 1004, II-232, II-234). As also indicated above in connection with claim 1, Petitioner provides multiple reasons to combine Zavracky, Chiricescu, and Akasaka, including to allow for speed and bandwidth gains and parallelism, and minimize reconfiguration and propagation delays, with a well-known desire to increase bus sizes. *See* Pet. 12, 18, 20; Reply 5–8. Petitioner also contends it would have been obvious to employ Chiricescu's cache memory teachings in the combined 3-D stack to reconfigure data in order to accelerate access to the external memory references of claim 1. *See* Pet. 32 ("Therefore, when the FPGA (i.e.,

the processing element) needs to be reconfigured, with new data, access to that data is accelerated by already having been loaded into the memory array." (citing Ex. 1004, II-234) (emphasis omitted).

Addressing claims 17 and 24, Patent Owner argues that "[t]he *Zavracky-Chiricescu-Akasaka* combination fails to teach or suggest a 3-D processor module that includes a second integrated die element, separate from a first integrated die element having a programmable array, wherein the 'memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.'" PO Resp. 24. Patent Owner states the "cited references" do not teach or suggest the "functional to accelerate external memory references" and "functional to accelerate reconfiguration" clauses, points to Petitioner's rationale with respect to claim 1 as discussed in the previous section (§ II.D.4), and concludes that claims 17 and 24 "are patentable." *Id.* at 24 (noting that "Petitioner relies on the same rationale for this claim element as it did for the element discussed directly above, i.e. 'memory array is functional to accelerate external memory references to said processing element'").

In other words, Patent Owner does not argue claims 1, 16, 17, 23, and 24 separately in a clear fashion. As noted above, claims 16 and 23 are materially the same as claim 1, and we address arguments with respect to claims 1, 16, and 23 (which Patent Owner groups together) above. *See supra* §§ II.D.4–5.

Patent Owner's argument with respect to claims 17 and 24, which essentially lists the limitations thereof and concludes that Petitioner fails to show

obviousness, does not undermine Petitioner's persuasive showing for these claims as summarized herein and also for the reasons discussed in this section and above in connection with claim 1 and other argued claims. As summarized above, Petitioner's showing that external memory references in the combined teachings of include data or other references for reconfiguring the FPGA is persuasive. *See* Pet. 31–33, 44–45, 49–50; *supra* §§ II.D.4–5.

We adopt and incorporate Petitioner's showing for claims 17 and 24, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14–22, 45, 49–50. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 17 and 24 would have been obvious.

7. *Claims 18–22*

Independent claim 18 is similar to claim 1 and recites a "reconfigurable processor module comprising" at least three integrated circuit elements including "a programmable array including a processing element," a processor electrically coupled thereto, and "a memory stacked with and electrically coupled" to both integrated circuit elements, "whereby said processor and said programmable array are operational to share data therebetween."

Addressing the three integrated circuit elements, Petitioner relies on its similar showing with respect to claims 1, 4 (third integrated circuit), 9 (third integrated circuit is a memory), and 10

(programmable array, processor, and memory electrically coupled with memory functional to accelerate external memory references). *See* Pet. 23–33, 35–36, 40–42, 45–46. Petitioner relies on Zavracky's disclosure of programmable logic array 802 (FPGA) in a stacked 3-D processor module with microprocessor layers 804 and 806 (Ex. 1003, Fig. 13), and Chiricescu's teaching of a 3-D chip comprising FPGA, memory, and routing layers (Ex. 1004, Fig. 2). *See id.* Further relying on Zavracky's Figure 13, Petitioner asserts that "each of the programmable array, microprocessor, and memory IC functional elements are pair-wise stacked with and electrically coupled with each other" through vertical vias and buses. *Id.* at 28–29 (also noting that Zavracky teaches that "[i]nter-layer connections . . . can be placed anywhere on the die" of the functional element(s), meaning the connections "are not limited to placement on the outer periphery" (quoting Ex. 1003, 6:43–7:9)). Petitioner also relies on Akasaka's teaching and suggestion that in a 3-D stack, "[e]ach active layer is connected electrically through via holes" (*id.* at 30 (quoting Ex. 1005, 1707)), and on similar motivation as for claim 1 (*see id.* at 18–22, 31–33, 48 (citing Pet. § VII.A.4; Ex. 1002 ¶¶ 233–239, 347–348)).

Addressing the claim 18 limitation "whereby said processor and said programmable array are operational to share data therebetween," Petitioner refers to Akasaka's disclosure of 3-D chips wherein "memory data are kept common by the interlayer (vertical) signal [so that] **each processor can use the common memory data**." Pet. 49 (emphasis by Petitioner) (quoting Ex. 1005, 1713). In addition, Petitioner argues that "the POSITA knew of the need

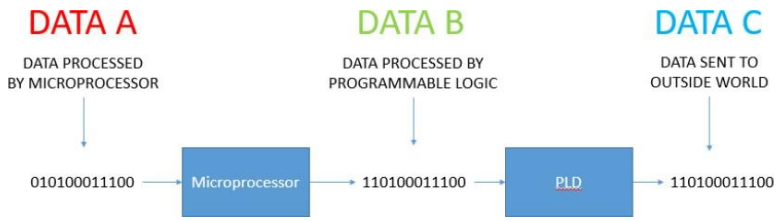
for replicated 'common data memory' in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence." *Id.* at 21 (citing Ex. 1002 ¶ 236; Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25). Petitioner further explains that "[t]hat structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky," further motivating "[a] POSITA . . . to seek out Akasaka's distributed contact points in order to build a "common data memory." *Id.* at 20 (citing Ex. 1002 ¶ 237).

Petitioner also relies on Akasaka's teaching that that "information signals can be transferred" through "several thousands or tens of thousands of via holes . . . present in these devices" to further suggest employing Akasaka's "thousands of via holes in the context of Zavracky" as further suggesting the claimed data sharing feature. Pet. 47–48 (first two quotes quoting Ex. 1005, 1705; citing Ex. 1002 ¶¶ 233–239, 347–348). As noted throughout this Final Written Decision, Petitioner also relies on known benefits of increased speed, bandwidth, and capability for parallel processing based on well-known teachings, to suggest stacking layers, including memory layers, using numerous vias, to combine the teachings of Zavracky, Chiricescu, and Akasaka. *See id.* at 8–9, 12, 17–22. For example, Petitioner states that "[t]he POSITA would have sought out Akasaka's connectivity to improve Zavracky's stacks in applications requiring parallel processing. Such applications included image processing algorithms [that] run simultaneously over an entire image in memory." *Id.* at 20–21 (Ex. 1002 ¶ 235; Ex. 1048; Ex. 1005; Ex. 1021).

Petitioner explains that Zavracky also teaches that its programmable logic 802 is an FPGA and serves as "an intermediary between 'the microprocessor and any off-chip resources.'" Pet. 47 (citing Ex. 1003, 12:28–36). Petitioner also relies on Zavracky's "[i]nterconnect lines" operating as a "data bus." *Id.* (quoting Ex. 1003, 6:39–42). According to Petitioner, a "POSITA would have recognized that communication between 'the microprocessor and any off-chip resources' via the FPGA (under the Zavracky-Chiricescu-Akasaka Combination as explained in [1.1], [1.2] and [2]) means that data is shared between the microprocessor and the FPGA." *Id.* (citing Ex. 1002 ¶ 342).

Claims 19–22 depend from independent claim 18. Claim 19 recites "wherein said memory is operational to at least temporarily store said data." *See* Pet. 48–49. Petitioner argues that "[t]he POSITA would have understood that memory is—by definition—operational to at least temporarily store data." *Id.* at 48 (citing Ex. 1002 ¶ 308 (citing Ex. 1039 (trade dictionary defining memory)). Petitioner also relies on Akasaka's shared memory as discussed above and further below in connection with claim 18. *See id.* (citing Ex. 1005, 1713). Petitioner asserts that the added claim limitations of claims 20–22, which depend from claim 18 and recite an "FPGA," a "microprocessor," and a "memory array," respectively, read on Zavracky's stack as depicted in Figure 13. *See id.* at 49 (relying on the analysis for claims 1, 2, and 10); *supra* § II.D.4 (analyzing claims 1, 2, and 10). In other words, Petitioner relies on its showing with respect to materially the same limitations in claims 1, 2, and 10 to address claims 20–22. Pet. 49. Patent Owner does not challenge claims 19–22 separately.

Addressing claim 18, Patent Owner argues that "[t]he *Zavracky* microprocessor and programmable logic are not operational to ***share*** data, such as might be stored in a stacked memory die, for example." PO Resp. 25 (citing Ex. 2011 ¶ 63). Patent Owner reproduces the following diagram from Dr. Souri's declaration to illustrate its point:



Ex. 1012 ¶ 63. According to Patent Owner, Zavracky's microprocessor on the left does not share data with the FPGA (PLD) on the right, because "it is the output of Zavracky's microprocessor that is sent to the FPGA." PO Resp. 25 (citing Ex. 1012 ¶ 63).

Patent Owner attempts to distinguish "sharing" data and "transferring" data by arguing that "[t]he claims require more than a processor transferring data to a field programmable gate array." *See* PO Resp. 25–26. Neither the '951 patent specification nor claim 18 requires this distinction. Nevertheless, Patent Owner argues that shared data "might be stored in a stacked memory die, for example." PO Resp. 25. Grouping claims 18–22 together, Patent Owner similarly argues in its Sur-reply that "[a] POSITA would recognize that this data on the stacked memory die is literally 'data shared between a microprocessor and an FPGA.'" Sur-reply 11–12 (citing Ex. 2011 ¶ 64; Ex. 1001, 2:1–9, 2:56–60, 5:18–29).

Contrary to this line of argument, claims 18–22 do not require a "stacked memory die" to hold data to support the recited shared data functionality. Although claim 19 recites "wherein said memory is operational to at least temporarily store said data," claim 19 is broad enough to read on Zavracky's modified memory (which is operational to store the shared data) *after* the microprocessor and FPGA (are operational to) share it per claim 18. *See* Pet. 48 (arguing that "[t]he POSITA would have understood that memory is—by definition—operational to at least temporarily store data" (citing Ex. 1002 ¶ 308 (citing Ex. 1039 (trade dictionary defining memory)).[18]

Moreover, even under Dr. Souri's diagram of Zavracky's process, Zavracky's microprocessor processes the input data to create the shared output data, and then transfers that shared output data onto the data bus and then to the FPGA. *See* Reply 13–14 (citing Ex. 1070 ¶¶ 73–74; Ex. 1083); Ex. 1070 ¶ 73 (quoting Ex. 1083, 1:26–34 (describing computers "shar[ing] data" by "transfer[ing] data")); Pet. 47–48 (citing Ex. 1002 ¶¶ 343–349). As discussed further below, Petitioner also persuasively explains how Zavracky's microprocessor and FPGA share and process the same data from off-chip resources to implement a user-defined protocol. *See* Pet. 47.

Patent Owner also argues that Petitioner's theory based on Akasaka's teaching and suggestion to

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[18] As indicated herein, Patent Owner does not address Petitioner's persuasive showing for claim 19 separately from claim 18. Petitioner also persuasively relies on Akasaka's shared memory for claims 18–22 as discussed further below. *See* Pet. 47–50 (citing Ex. 1005, 1713).

share "'common memory data' does not cure this fundamental deficiency in *Zavracky* because it also does not involve any processing of data shared between a microprocessor and an FPGA (or any other type of chip)." PO Resp. 26. Claims 18–22 do not require "processing of [shared] data," but even if the claims imply that interpretation, the combined teachings suggest it, as Petitioner persuasively shows as discussed next.

To support its point, Patent Owner reproduces *Akasaka's* Figure 25 as follows:

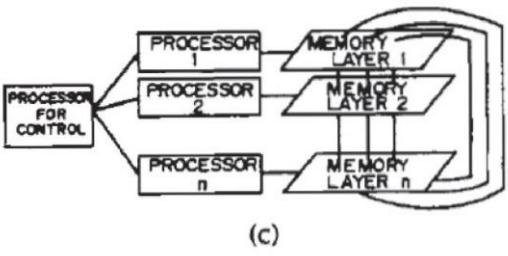

Fig. 25. New concept of 3-D IC. (a) 3-D PLA model (by Prof. T. Nanya of the Tokyo Institute of Technology). (b) Integration of CAM RAM in the same chip (by T. Ogura of NTT). (c) Common memory data system for 3-D memory chip (by Prof. M. Hirose of Hiroshima University).

PO Resp. 27. Figure 25(c) above depicts a "[c]ommon memory data system for a "3-D memory chip" wherein processors 1, 2, n (on the left) share data on memory layers 1, 2, n (on the right). Ex. 1005, 11. Akasaka states that "memory in each chip belongs to corresponding independent microprocessors in the same layer, *and the memory data are kept common by the interlayer (vertical signal) transfer*." *Id.* (emphasis added).

Patent Owner argues that "although *Akasaka* proposes that memory data is 'kept common by the interlayer (vertical) signal transfer,' the individual microprocessors do not process any shared data because each only processes the data in its corresponding memory." PO Resp. 27. This argument misses the mark, because Akasaka's system transfers the same data between the memories so that each processor is operational to process the same data. Stated differently, Akasaka contradicts Patent Owner's argument that transferring the same data at one memory location (the "common" data in Akasaka) to another memory location shows a lack of data sharing—i.e., Akasaka describes the data as "common." *See* Ex. 1005, 11.

As to sharing data between a processor and an FPGA, Petitioner relies on Akasaka's teaching as suggesting the sharing of common data through vertical data transfers in the combined 3-D structure of Zavracky, Chiricescu, and Akasaka, instead of relying on a bodily incorporation of the processor memory layer scheme of Akasaka. *See* Pet. 47–48; Reply 14 (arguing that Patent "attacks the physical die-stacking technique in Akasaka—but Zavracky already teaches stacked memories that are interconnected to other dies in the stack, and also teaches memories can be at any layer" (citing Ex. 1003, 11:63–12:2, Figs. 10, 12)). Claims 18–22 are agnostic as to how the FPGA and microprocessor share data—i.e., with or without a separate memory in each layer—i.e., claim 18 recites "whereby said processor and said programmable array are operational to share data therebetween" without reference to the "memory" recited earlier in the claim.

As proposed by Petitioner, it would have been obvious for the FPGA and microprocessor of Zavracky-Chiricescu, based on Akasaka's teachings, to share data using numerous (e.g., thousands) of vertical vias to implement the data transfer and thereby increase processing speeds and bandwidth. *See* Pet. 47–48 (citing Pet. § VII.A.4 (reasons to combine the references); Ex. 1002 ¶¶ 233–239; 347–348). For example, as Petitioner shows, using Akasaka's teachings, including its memory teachings to share data using thousands of vertical vias would have "increase[d] bandwidth and processing speed through better parallelism and increased connectivity." *See* Pet. 20 (citing Ex. 1002 ¶ 233; Ex. 1005, 1705); Reply 6–7 (citing known advantages of numerous vertical vias). Petitioner also persuasively shows that skilled artisans would have recognized that using Akasaka's memory teachings and dense via structure allows for increases in processing speed and improved parallelism and ensures cache coherency in the modified stack of Zavracky. *See id.* at 20–21 (citing Ex. 1002 ¶¶ 236–237; Ex. 1005, 1705, 1713).

Patent Owner's arguments do not address Petitioner's more general showing that a "POSITA would have recognized that communication between 'the microprocessor and any off-chip resources' via the FPGA (under the Zavracky-Chiricescu-Akasaka Combination as explained in [1.1], [1.2] and [2]) means that data is shared between [and processed by] the microprocessor and the FPGA." *See* Pet. 47 (citing Ex. 1002 ¶¶ 342–346). In other words, Dr. Souri's diagram above only refers to data *from* the PLD (FPGA) as "DATA SENT TO THE OUTSIDE WORLD," but this analysis does not address Petitioner's persuasive showing that data from the

outside world (off-chip) passes through the FPGA as an intermediary to the microprocessor. *See* Pet. 48–49 (quoting citing Ex. 1003, 12:28–36). At the cited passage, prior to describing Figure 13, Zavracky states that "[p]rogrammable logic arrays can be used to provide communication between a multi-layered microprocessor and the outside world." Ex. 1003, 12:29–31. Zavracky also states that "programmable logic array 802 [an FPGA in Figure 13] can be programmed to provide for user-defined communications protocol between the microprocessor and any off-chip resources." *Id.* at 12:36–37. Figure 13 shows bus connections on the PLD 802 (FPGA) to the outside world, with bus connections from PLD 802 to microprocessor 804/806 and memory 808. *See* Ex. 1003, Fig. 13, 12:29–39. Therefore, as Petitioner argues, Zavracky shows that communication occurs between the microprocessor and the FPGA, thereby teaching the sharing of data between the two (in at least one of the two directions). *See* Pet. 48–49.

In addition, in advancing another argument, Patent Owner admits that the combination teaches data sharing: "[T[he approach of Zavracky- Chiricescu would result in a structure in which *data is removed from the microprocessor cache and placed in the FPGA's on-chip memory*," and "*data . . . might be shared* between *Chiricescu's* FPGA and *Zavracky's* microprocessor." PO Resp. 29 (emphasis added).

Patent Owner also argues that "to modify the *Zavracky-Chiricescu* system with *Akasaka*, . . . the ***stacked*** memory layer of *Chiricescu* would need to be moved into its RLB layer because *Akasaka* requires each memory layer to be located on the same layer as its associated processor," thereby requiring a "major

modification" of Chiricescu. PO Resp. 37. Patent Owner similarly argues that implementing the combination requires "adding ***more*** structure to *Chiricescu's* RLB layer, in the form of *Akasaka's* memory, destroys *Chiricescu's* principle of operation, which relies on moving as much structure ***out of*** the RLB layer as possible." *Id.*

This line of argument incorrectly assumes that Petitioner must show how to bodily incorporate the common memory teachings of Akasaka into Chiricescu's structure as part of its obviousness showing. This argument is unavailing, because Petitioner relies on Zavracky's 3-D stack structure, including its memory as a separate layer and on Akasaka's thousands of via holes, informed by the common memory teachings of Akasaka, without any modification to Chiricescu's FPGA teachings required. The common memory teachings of Akasaka are agnostic as to the memory location.

That is, Akasaka does not "require[] each memory layer to be located on the same layer as its associated processor." *See* PO Resp. 37. Even though Figure 25 of Akasaka shows a stack of processors and memory, with a processor and memory on the same layer, nothing in Akasaka states that the memory cannot be elsewhere in the stack on a separate layer. Rather, Figure 25 shows all memories connected together electrically with each memory connected electrically to its respective processor. *See* Ex. 1005, Fig. 25. These electrical connections suggest to an artisan of ordinary skill that the memory layer's location is less important than the electrical connections. *See id.* Moreover, Petitioner relies on Zavracky's separate layer for each memory in a stack with via connections

to enhance speed, as the combination suggests. *See* Reply 14 ("Zavracky already teaches stacked memories that are interconnected to other dies in the stack, and also teaches memories can be at any layer" (citing Ex. 1003, Figs. 10, 12, 11:63–12:2 ("[A]n additional layer or several layers of random access memory may be stacked. . . . This configuration results in reduced memory access time, increasing the speed of the whole system")).

We adopt and incorporate Petitioner's showing for claims 18–22, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14– 22, 46–49. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 18–22 would have been obvious.

8. *Summary*

After a full review of the record, including Patent Owner's Response and Sur-reply and evidence, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, and Akasaka would have rendered obvious claims 1, 2, 4–6, 8–24, 27, 29.

E. *Obviousness, Claim 25*

1. *Trimberger*

Trimberger, titled "A Time-Multiplexed FPGA" (1997), describes an FPGA with on-chip memory distributed around the chip. Ex. 1006, 22. Trimberger teaches that the memory "can also be read and written by on- chip [FPGA] logic, giving applications access to a single large block of RAM." *Id.* Trimberger teaches

this "storage [can] be used as a block memory efficiently." *Id.* at 28.

Trimberger's Figure 1 follows:

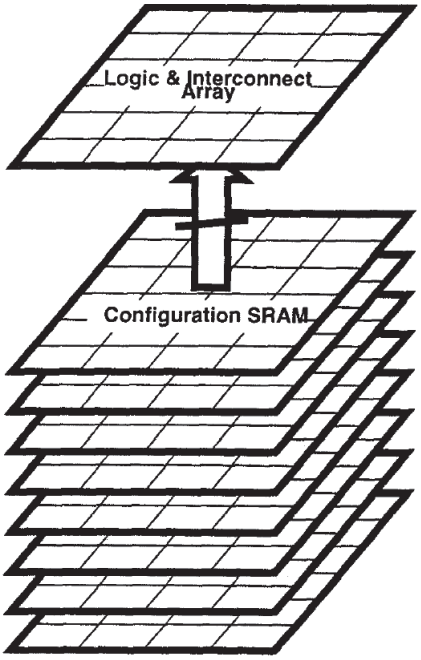

Figure 1. Time-Multiplexed FPGA Configuration Model

Figure 1 of Trimberger above depicts eight planes of SRAM (static random access memory) for an FPGA. *See* Ex. 1006, 22–23. "The configuration memory is distributed throughout the die . . . . This distributed memory can be viewed as eight *configuration memory planes* (figure 1). Each plane is a very large word of memory (100,000 bits in a 20x20 device)." *Id.* at 22.

Trimberger also teaches accessing each plane of memory as one simultaneous parallel transfer of 100,000 memory data bits to reconfigure the FPGA quickly: "When the device is *flash reconfigured* all bits in logic and interconnect array are updated

simultaneously from one memory plane. This process takes about 5ns. After flash reconfiguration, about 24ns is required for signals in the design to settle." Ex. 1006, 22.

2. *Claim 25*

Dependent claim 25 recites "[t]he programmable array module of claim 23 wherein said memory array is functional as block memory for said processing element." Petitioner contends that claim 25 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. Pet. 52–55.

Petitioner relies on Trimberger's block memory teachings to address claim 25. *See* Pet. 58–60. According to Petitioner,

> Trimberger teaches that its co-located "memory is **accessible as block RAM** for applications," that are running in the FPGA, i.e., that the memory "can also be read and written by on-chip [FPGA] logic, giving applications access to a single large block of RAM." Ex. 1006, 22. Trimberger teaches that "the configuration storage to be used **as a block memory efficiently**." [*Id.* at 28].

Pet. 55 (emphasis by Petitioner) (quoting Ex. 1006, 22, 28). Petitioner contends that it would have been obvious to employ Trimberger's block memory to support fast local memory in FPGA applications like that in the combined teachings of Zavracky, Chiricescu, and Akasaka, with "the memory stacked and electrically coupled nearby." *See id.* at 53–55 (citing Ex. 1002 ¶¶ 247–256; Ex. 1020; Ex. 1048). Petitioner also contends that "[t]he POSITA would have known that FPGAs have limited programmable

logic space, and that for certain tasks it would be more cost efficient and silicon-efficient to use the FPGA for reconfigurable processing and to use a separate task-dedicated memory element for block memory." *Id.* at 54 (citing Ex. 1002 ¶ 247). Petitioner advances other reasons for the combination. *See id.* at 54–55 (characterizing Trimberger's on-chip block memory as faster relative to off-chip memory).

Patent Owner argues that "[d]ependent [c]laim 25 requires the "the 'block memory' and 'field programmable gate array' to be on ***different*** chips." PO Resp. 44. According to Patent Owner "*Trimberger* . . . teaches away from having its block memory and FPGA on different chips as it attributes its quick FPGA reconfiguration to the massive connectivity ***within*** the chip." *Id.* (citing Ex. 1006, 22; Ex. 2011 ¶ 88); *see also id.* at 50– 51 (same argument (citing Ex. 2011 ¶ 97)). Patent Owner primarily relies on this "within the chip" or "on-chip memory" argument as the basis for its allegations of lack of motivation, lack of reasonable expectation of success, teaching away, requirement for major modifications, and other related arguments. *See id.* at 43–51.

For example, Patent Owner argues that "implementing Trimberger's FPGA structure in Xilinx's combination would result in a complete redesign of the hypothetical 3-D stacked structure of the *Zavracky-Chiricescu- Akasaka* Combination," because "the block memory is no longer stacked with the FPGA, but instead located on *Trimberger's* FPGA die as on-chip memory." PO Resp. 49 (citing Ex. 2011 ¶ 95). Patent Owner explains that "*Trimberger's* FPGA structure requires that its configuration memory planes are located on the same die as the

FPGA's logic cells, so that the FPGA can quickly switch between different configurations." *Id.* at 50 (citing Ex. 2011 ¶ 97). Patent Owner asserts that "Petitioner admits this." *Id.* (citing Pet. 53 (characterizing the Petition as stating that Trimberger teaches a time multiplexed FPGA with on-chip memory distributed around the chip)). Based on these assertions, Patent Owner contends that evidence lacks as to "how or why a POSITA would have had a reasonable expectation of success in making the combination." *Id.* at 45; *see also id.* at 49–51 (similar arguments).

Petitioner persuasively shows that Trimberger does not teach away or support Patent Owner's related arguments based on the single-chip theory, including hypothetical re-designs, and lack of a reasonable expectation of success and motivation. Petitioner does not admit that Trimberger "*requires* that its configuration memory planes are located on the same die as the FPGA's logic cells." *See* PO Resp. 50 (citing Pet. 53); Pet. 53 (describing Trimberger's on-chip memory without characterizing it as a requirement).

Petitioner persuasively points out that Trimberger does not "criticize, discredit, or otherwise discourage investigation into the invention claimed," merely because it discloses embodiments having block memory and an FPGA within the same chip. Reply 22 (quoting *Depuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009)). Petitioner persuasively argues that Patent Owner's "'massive connectivity' observations about Trimberger confirm that the POSITA would have been further encouraged to make the combination." *Id.* at 23 (citing

Ex. 1070 ¶¶ 44–45); *see* PO Resp. 50 (arguing Trimberger's block memory includes "massive connectivity" with the FPGA).

Petitioner's response, supported by Dr. Franzon's testimony, is persuasive. Trimberger's Figure 1 shows eight different memory planes on a single chip. Ex. 1006, 22. Trimberger states that "[t]he entire configuration of the FPGA can be loaded from this on-chip memory in 30ns." *Id.* Trimberger does not teach, and Dr. Souri does not testify, that Trimberger's "on-chip memory" *requires* each memory plane to be on *the same layer* as the FPGA of a chip, such as a multi-layered chip or stack of chips. *See id.*; Ex. 2011 ¶ 97 (describing Trimberger as employing "massive connectivity ***within*** the chip").

Dr. Franzon explains credibly that "Trimberger's one-cycle teachings would be **improved** by applying its teaching to a 3D chip." Ex. 1070 ¶ 44. Dr. Franzon explains that Trimberger's reconfiguration clock cycle "(i.e., the delay in Trimberger) is set [by] determin[ing] the length of the longest path after routing." *Id.* (quoting Ex. 1006, 27). Then, Dr. Franzon testifies that "[t]he point here is that a shorter vertical interconnect allows for a shorter 'longest path' and a faster chip" and "[t]his was commonly understood in the other art." *Id.* (noting that "Akasaka taught that 3-D 'high speed performance' was enhanced because '[i]n 2-D ICs, the longest signal interconnection length becomes several to ten millimeters, but in 3-D ICs the length between upper and lower layers is on the order of 1–2 μm.'" (quoting Ex. 1005, 1705); also noting that Zavracky teaches that **"[i]n the proposed approach, shorter busses will result in smaller delays and higher speed circuit performance**"

(quoting Ex. 1003, 3:4–14) (emphasis by Dr. Franzon)).

This testimony goes hand-in-hand with Petitioner's showing as summarized above in connection with the challenged claims discussed above. That is, Petitioner shows persuasively that the combined teachings of Zavracky, Chiricescu, and Akasaka suggest short conductor runs using numerous distributed vias of a 3-D multi-layer chip to increase speed and bandwidth, decrease path delays, and facilitate parallel processing. *See supra* § II.D.4–7; Pet. 7–9, 17–22 (background knowledge of an artisan of ordinary skill includes stacking chips with multiple distributed vias to minimize latency, interconnection delay, and reconfiguration times, allow for parallel processing, and increase operating speed, etc.). The Petition also persuasively points to a "concern[] with the speed of access between the FPGA and the block of memory" as a reason to use Trimberger's "block memory . . . combined with Zavracky-Chiricescu-Akasaka's teaching of having the memory stacked and electrically coupled nearby." Pet. 54.

Supported by Dr. Franzon's testimony, Petitioner also persuasively responds that arranging a block memory on a separate layer from an (FPGA) processing element is not a major modification and the evidence shows how to do it would have been well within the level of ordinary skill. *See* Reply 23–24; Ex. 1070 ¶ 46 ("Dr. Souri does not understand the combination being made. The Zavracky, Chiricescu, Akasaka combination already has a memory and an FPGA. It is already connected via a wide-area

distributed set of interconnections as taught in Akasaka.").

Petitioner persuasively points to the Petition as stating that "[t]he POSITA would have sought Trimberger's teaching of using memory as a block memory and combined that with Zavracky-Chiricescu-Akasaka's teaching of **having the memory stacked and electrically coupled nearby**." Reply 23 (citing Pet. 54). In other words, Petitioner does not propose "'***moving***' *Trimberger's* on chip memory" to the same layer as the FPGA in Zavracky-Chiricescu-Akasaka's 3-D stack, contrary to Patent Owner's argument. *See* PO Resp. 50; Sur-reply 20. Rather, Petitioner proposes modifying the existing memory of Zavracky's modified 3-D stack to function as a block memory according to Trimberger's teachings. *See* Pet. 54; Reply 24. Moreover, Trimberger's eight plane memory design suggests different layers at least for each plane of memory, and challenged claim 25 does not require more than one of Trimberger's block memory planes. *See* Pet. 54 (describing "us[ing] a separate task-dedicated memory element for block memory"); Ex. 1006, Fig. 1 (showing eight different time multiplexed memory planes); Ex. 1070 ¶ 45 (testifying that in Trimberger's Figure 1 (*see supra* § II.E.1), "the fat arrow with a line in the traditional representation of 'many signals' – i.e., this is suggesting an architecture where different 'planes of memory' (i.e., layers of a die in a stack) are transferred from the configuration SRAMs to the FPGA").[19]

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[19] As summarized above, each memory plane in Trimberger contains 100,000 bits of memory. *Supra* § II.E.1. Also, "[w]hen the device is *flash reconfigured* all bits in logic and interconnect

In any event, claim 25 does not preclude eight separate memory layers in a stack, or all eight memory planes on the same layer in the stack, or a multiplexor to select the different memory planes. Patent Owner essentially argues that an artisan of ordinary skill can connect eight memory planes to an FPGA on a single layer, but cannot do the same with vias on separate layers with a reasonable expectation of success. The record shows otherwise, for the reasons outlined above.

Petitioner persuasively points to testimony by Dr. Franzon cited in the Petition, who in turn relies credibly on evidence of record, to show a reasonable expectation of success, showing that implementing block memory with an FPGA was well-known in the prior art. *See* Reply 24 (citing Pet. 57; Ex. 1002 ¶ 145, 248; Ex. 1003, Figs. 12, 13; Ex. 1003, 11:63–12:2; Ex. 1002 ¶145); Ex. 1002 ¶ 145 (testifying that "Cooke also discloses that the 'memory planes not being used for configuration may be used as memory,' i.e., an extra memory block for use by the FPGA" (citing Ex. 1032), ¶ 144 (testifying that Casselman shows connecting "memory . . . directly to FPGA . . . through address and data busses." (citing Ex. 1026)).

As discussed above in connection with challenged claims 1, 2, 4–6, 8– 24, 27, and 29, Petitioner persuasively outlines several good reasons to combine related teachings from the references to arrive at a 3-

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array are updated simultaneously *from one memory plane*. *Id.*; Ex. 1006, 22 (emphasis added). Contrary to Patent Owner's arguments in connection with claims 1 and 23– 25 discussed above, Trimberger provides another example of the prior art showing the connection of a large plane of memory (block memory) directly to an FPGA for reconfiguration in one cycle.

D stack that includes memory, FPGA, and a processor, reasons that apply to Trimberger's block memory. *See supra* § II.D.4–7; Pet. 7–9, 17–22, 55–57. For example, Petitioner notes that Trimberger teaches a block memory to provide access to a "single large block of RAM" such that memory "can . . . be read and written by on-chip [FPGA] logic." Pet. 56 (quoting Ex. 1006, 22). Petitioner also states that implementing Trimberger's block memory teachings with the 3-D chip combination as suggested by Zavracky's "stack [of] memories together with processors or the programmable array" addresses "concern[s] *with the speed of access* between the FPGA and the block memory." *See id.* at 57 (emphasis added). Petitioner notes that "FPGAs have limited programmable logic space" suggesting "a separate task-dedicated memory element for block memory." *Id.* Petitioner also persuasively argues that applying Trimberger as a separate layer (or layers) of memory in the 3-D stack of Zavracky, Chiricescu, and Akasaka "would have merely been a combination of prior art elements according to known methods to yield a predictable result" and "would have been a well-known use of a memory," showing a reasonable expectation of success in "improv[ing] on the memory options of the FPGA." *Id.* As outlined above, the record supports Petitioner.

Patent Owner repeats or repackages its arguments addressed above, by arguing that "Trimberger does not cure any of the aforementioned deficiencies," "*Chiricescu* does not employ *Zavracky's* interconnections to connect a memory die to an FPGA die," and Petitioner does not show why or how "the modification would have been achieved with any reasonable expectation of success." *See* PO Resp. 46.

Contrary to these arguments, as outlined above, Petitioner relies on the combined teachings of the references and the knowledge of an artisan of ordinary skill, and Trimberger provides more and persuasive evidence as to how and why an artisan of ordinary skill would have employed block memory as a single plane or several planes as separate layers in a 3-D stack, including to enhance reconfiguration speeds between a large block of memory and FPGA by facilitating a large parallel data transfer of 100,000 bits in one clock cycle.

We adopt and incorporate Petitioner's showing for claim 25, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14– 22, 52–55. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Trimberger would have rendered obvious claim 25.

F. *Obviousness, Claim 26*

1. *Satoh*

Satoh, titled "Semiconductor Integrated Circuit, Method for Testing the Same, and Method for Manufacturing the Same," describes using an FPGA to generate test stimuli to test memory elements on the same chip. Ex. 1008, code (54). In one embodiment, Satoh describes

> a method for testing this semiconductor integrated circuit is such that, in a semiconductor integrated circuit incorporating a variable logic

> circuit (FPGA) for outputting a signal indicating whether or not a circuit is normal [wherein] . . . a memory test circuit is built for testing the memory circuits in accordance with a specified algorithm . . . without using an external high-performance tester.

Ex. 1008, 46.[20]

Satoh also describes a "memory array" and testing DRAMs (dynamic random access memory arrays) such that "a test circuit . . . for testing the DRAMs 150 to 180 is formed in the portion of the FPGA 120 . . . , and the DRAMs 150 to 180 are tested in succession." *See* Ex. 1008, 15, Fig. 7.

2. *Claim 26*

Dependent claim 26 recites "[t]he programmable array module of claim 23 wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element." Petitioner contends claim 26 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Satoh. *See* Pet. 60–63.

Petitioner contends that "[i]t was well-known to test stacked modules in order to avoid the expense and waste of silicon by creating 'dead' chips, and improve yield." Pet. 57 (citing Ex. 1002 ¶ 241; Ex. 1009; Ex. 1043). Petitioner states that "Satoh specifically praised the use of an FPGA to test 'memory circuits' for 'improving yield and productivity of the

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[20] Page citations refer to original page numbers.

semiconductor integrated circuit.'" *Id.* (quoting Ex. 1008, 47:23–27).

Petitioner explains that Satoh describes an FPGA that "generates a specified test signal [and] supplies the test signal to the memory circuit." Pet. 58 (citing Ex. 1002 ¶¶ 350–359; Ex. 1008, 5:1–28, 49:32–37). Petitioner maintains that Satoh's test signal suggests a "test stimulus" to a second integrated circuit memory array to evoke a response therefrom. *See id.* (citing Ex. 1008, 49:32–37; Ex. 1002 ¶ 358). Based on Satoh's teaching, Petitioner explains that "[i]n the Zavracky-Chiricescu-Akasaka-Satoh Combination," it would have been obvious to implement "the test signal . . . through the contact points between the FPGA of the first IC functional element and the memory of the second IC functional element," because that "is how those elements are stacked and electrically coupled." *See id.* (citing Ex. 1002

¶ 359).

In addition to avoiding "dead chips," Petitioner cites other reasons to combine Satoh's testing functionality with the 3-D chip of Zavracky-Chiricescu-Akasaka:

> Recognizing the need to test the 3D stack of the Zavracky- Chiricescu-Akasaka Combination, the POSITA would have sought out Satoh's teaching of using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity. Ex. 1002 ¶242. Moreover, (4) a FPGA is reusable:

> after being configured for testing in manufacture, the FPGA would then be reconfigured for its normal "in the field" purpose. *Id.* (citing Ex. 1045 ("Another advantage . . . is that after testing is complete, the reconfigurable logic (FPGA 28) can be reconfigured for post- testing adapter card functions."); Ex. 1046).

Pet. 57.

Petitioner also relies on the following evidence and rationale to support a reasonable expectation of success:

> It was well known to use a FPGA to test circuitry with 2-D chips as taught by Satoh. Ex. 1002 ¶241 (citing Ex. 1043). The POSITA would have recognized Satoh's teaching would readily apply to the 3-D chip elements in the Zavracky-Chiricescu- Akasaka Combination. This includes because such a combination would have been a routine use of an FPGA, whose testing ability was not dependent on structure. Ex. 1002 ¶¶242–43. The result of this combination would have been predictable, by known FPGA testing to the 3D stack according to known methods to yield a predictable result. Ex. 1002 ¶244.

Pet. 57–58.

Patent Owner relies on the same unavailing arguments it advances with respect to the challenged claims addressed above. *See* PO Resp. 51–52 ("Because Petitioner does not contend that *Satoh* cures any of the deficiencies of the combination of *Zavracky*, *Chiricescu,* and *Akasaka,* as discussed above with respect to Ground 1, its reliance on the same rationales for Ground 3 also fail.").

Patent Owner also argues that "Petitioner's contention that a POSITA would be motivated to make the combination because it was well-known to test stacked die and *Satoh* tested memory elements on the same semiconductor chip (*see* Petition at 57) is divorced from the claimed invention." PO Resp. 52. Patent Owner contends that "Petitioner's generic rationale for using FPGAs for testing is wanting in particularity as to why a POSITA would combine the references as recited in the Challenged Claim." *Id.* Patent Owner contends that "[w]hether the use of *Satoh's* FPGA is beneficial for testing does not sufficiently explain why a POSITA would have combined the references to yield the claimed invention." *Id.* at 53. Patent Owner contends that Petitioner's rationale fails "as it lacks sufficient explanation of how or why a POSITA would have been motivated to use *Satoh's* FPGA for testing with the hypothetical 3-D structure of *Zavracky- Chiricescu-Akasaka* 'in the way the claimed invention does.'" *Id.* (quoting *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012)).

Patent Owner's arguments appear to accept Petitioner's showing that applying Satoh's testing structure and technique in "the hypothetical 3-D structure of *Zavracky-Chiricescu-Akasaka*" would have been "beneficial" and "predictable." *See* PO Resp. 52–53. That is, Patent Owner characterizes the rationale as "generic" without disputing it. *See id.*

In any event, Petitioner provides specific reasons related to specific recitations in the claims as outlined above, including tying Satoh's testing of a memory array using FPGA testing circuitry to the similar claim elements in claim 26. For example, using

Satoh's FPGA test circuitry and memory testing teachings to avoid "dead chips" is a specific "beneficial" reason, and tying these teachings to FPGA contact points in the Zavracky-Chiricescu-Akasaka stack to test memory in that stack also is specific. *See* Reply 24–25 (re-listing reasons supplied in the Petition, including, for example, "the known problem of the need to test stacked modules to avoid the expense and waste of silicon by creating 'dead' chips" (citing Ex. 1002 ¶ 241; Ex. 1009; Ex. 1020; Ex. 1043); Pet. 63 (explaining that "[i]n the Zavracky-Chiricescu- Akasaka-Satoh Combination, the test signal is sent through the contact points between the FPGA of the first IC functional element and the memory of the second IC functional element, which is how those elements are stacked and electrically coupled" (citing Ex. 1002 ¶ 359)). As Dr. Franzon also credibly explains, Satoh's use of generating a test signal "*within* an FPGA" to test a memory array is agnostic "to the particular way in which the FPGA is stacked." *See* Ex. 1002 ¶ 245 ("The POSITA would thus have realized that Satoh could be used to solve the existing need (which was also recognized by Ex. 1043, for example) to achieve the benefits discussed above.").

In other words, Petitioner persuasively shows a reasonable expectation of success with specific reasons to combine, all supported by the record, including beneficial testing to avoid dead chips and maintain reliable memory to reconfigure the 3-D stack's FPGA post-manufacture, thereby showing how to apply the teachings to the claimed 3-D stack as suggested by Zavracky, Chiricescu, and Akasaka. Specifically, claim 26 recites "wherein said contact points are further functional to provide test stimulus

from said [FPGA] to said at least second integrated circuit die element," and Petitioner persuasively applies Satoh's teachings to these contact points in order to avoid dead chips. Another set of specific and persuasive reasons to combine is "using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity." Pet. 57.

As Petitioner also persuasively argues, Petitioner's "evidence-backed assertions are uncontroverted, specific to relevant teachings of the references, and explain why a POSITA would have sought the Zavracky- Chiricescu-Akasaka-Satoh Combination to reach the '951 patent's claims." Reply 25 (citing Ex. 1070 ¶¶ 76–77).

Patent Owner advances a new (unresponsive) argument in its Sur- reply that "[t]he references Petitioner and Dr. Franzon cite do not disclose testing of 3D stacked processor but instead disclose that individual die are tested independently and prior to any 3D packaging." Sur-reply 22. This argument is not relevant to a claim limitation at issue here. Claim 26, a device claim, does not recite packaging, and it does not preclude "provid[ing] test stimulus from said field programmable gate array to said at least second integrated circuit die element" prior to any packaging.

We adopt and incorporate Petitioner's showing for claim 26, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14– 22, 55–58. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the

format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Satoh would have rendered obvious claim 26.

G. *Obviousness, Claim 28*

1. *Alexander*

Alexander, titled "Three-Dimensional Field-Programmable Gate Arrays" (1995), describes "stacking together a number of 2D FPGA bare dies" to form a 3-D FPGA. Ex. 1009, 253. Alexander explains that "each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die." *Id.*

Alexander's Figure 2 follows:

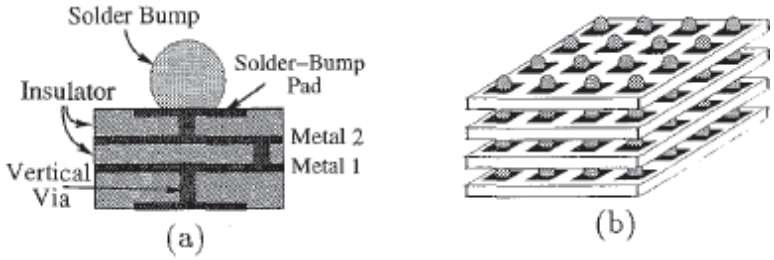

Figure 2: (a) The solder bump, pad, and vertical via geometry; and (b) stacked 2D FPGA dies.

Figure 2(a) shows vertical vias traversing a chip with a solder pad and solder bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1009, 253.

Alexander explains that stacking dies to form a 3-D FPGA results in a chip with a "significantly smaller physical space," lower "power consumption,"

and greater "resource utilization" and "versatility" as compared to conventional layouts. Ex. 1009, 253.

2. *Claim 28*

Dependent claim 28 depends from dependent claim 27, which depends from independent claim 23, and recites "[t]he programmable array module of claim 27 wherein said third integrated circuit functional element includes another field programmable gate array." As noted above, independent claim 23 is materially the same as independent claims 1 and 16. *Supra* § II.D.4; Pet. 49–50 (relying on its analysis for claims 1 and 16 to address claim 23). Dependent claim 27 involves materially the same analysis as claim 4 (also analyzed above), and recites "[t]he programmable array module of claim 23 further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements." *See* § II.D.5; Pet. 50 (relying on the showing for claim 4 to address claim 27).

Accordingly, claim 28 essentially adds another FPGA to claims 23 and 27 as addressed above, requiring at least three stacked integrated circuit die elements: a memory array stacked with "another" FPGA (i.e., a total of two FPGAs), with the "integrated circuit functional elements," which "include[]" the memory array and two FPGAS, electrically coupled together by "a number of contact points distributed through the surfaces of said functional elements," "wherein said memory array is functional to accelerate external memory references to said processing element [one of the FPGAs]" (as recited in independent claim 23).

Petitioner contends that claim 28 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Alexander. *See* Pet. 59–61. Addressing the two stacked FPGAs, Petitioner relies on Alexander's teaching of stacked FPGAs in a 3-D package, and contends as follows:

> The POSITA would have known (as Zavracky notes) that multiprocessor systems were needed for "parallel processing applications," for example, "signal processing applications." Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶258. But in this context, the POSTIA would have appreciated Alexander's teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). The POSITA would have sought out Alexander's multiple stacked FPGAs to enhance the Zavracky-Chiricescu-Akasaka Combination by upgrading it for this type of application. Ex. 1002 ¶259.

Pet. 60.

Petitioner contends that Alexander's similar structure of multiple stacked FPGAs, as similar to multiple processors stacked with multiple memories of the Zavracky-Chiricescu-Akasaka Combination, evidences a reasonable expectation of success of stacking FPGAs with memories, "with multiple functional elements stacked and vertically interconnected including using thousands of contact point vias (holes)." *See* Pet. 60. Petitioner also asserts that "[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to

known methods to yield a predictable result." *Id.* at 61 (citing Ex. 1002 ¶¶ 260–261).

Patent Owner responds that "[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no bearing on whether a POSITA would have been motivated to combine *Alexander* with *Zavracky-Chiricescu-Akasaka* to reach a 3-D processor module having 'a third integrated circuit functional element [that] includes another field programmable gate array.'" PO Resp. 54–55 (citing Ex. 2011 ¶ 100). This argument appears to accept Petitioner's showing that FPGAs are preferable to processors in a 3-D stack. Petitioner's unchallenged showing of faster FPGAs relative to general purpose processors in the 3-D stack of Zavracky-Chiricescu-Akasaka, where Zavracky contemplates multiple layers of processors, memory layers, and an FPGA, is a persuasive reason for the combination. *See* Ex. 1003, Fig. 12 (stacked multiple processor and memory layers/chips), Fig. 13 (stacked processor, memory, and PLA/FPGA layers/chips).

Patent Owner also argues that Petitioner's "conclusory rationale is further discredited by Petitioner's suggestions elsewhere in the Petition that *Chiricescu* discloses a FPGA application that enhances *Zavracky*." PO Resp. 55 (citing Pet. 19). In particular, Patent Owner argues that the Petition elsewhere suggest that a "POSITA would have taken Chiricescu's suggestion of a FPGA to perform 'arbitrary logic functions,' . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in *Zavracky*, e.g., to perform image and signal processing tasks that would have taken advantage of co-stacked microprocessors

and memories as taught in *Zavracky*." *Id.* (quoting Pet. 18). Patent Owner argues that "there is no reason . . . to combine *Alexander* with *Zavracky-Chiricescu-Akasaka*," because "Petitioner acknowledges that, *Chiricescu*, like *Alexander*, offers FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor." *Id.* (citing Ex. 2011 ¶ 101).

Patent Owner's arguments are unavailing. For example, Patent Owner concedes that "*Chiricescu*, like *Alexander*, offers FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor." PO Resp. 55. Claim 28 does not preclude employing a microprocessor, because it is open-ended and recites "comprising" and "at least" a "first," "second," and "third" "integrated circuit functional element." Petitioner specifically and persuasively argues that "[t]he POSITA would have known (as Zavracky notes) that *multiprocessor* systems were needed for 'parallel processing applications,' for example, 'signal processing applications.'" Pet. 60 (citing Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶ 258). And Petitioner repeatedly points to Zavracky's microprocessor in Figure 13 to address claim 1, and refers to this showing in addressing claim 23. *See* Pet. 23–24 (reproducing and annotating Zavracky's Figs. 12 and 13), 27 (addressing limitation [1.2], stating that "Figure 13 shows memory 808 and microprocessor 804 and 806 stacked above the programmable array"); Pet. 50 (addressing claim 23 and referring to "analysis in [1.2]"). Therefore, Patent Owner's characterization that Chiricescu and Alexander "offer[] FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor" and Petitioner's argument that

Chiricescu suggests FPGAs for performing arbitrary logic functions and expanding packet processing tasks with microprocessors, are specific and persuasive reasons to employ FPGAs in the stack of Zavracky-Chiricescu-Akasaka-Alexander. PO Resp. 55; Pet. 19. So too is simply replacing one or more of Zavracky's microprocessors with one or more preferable FPGAs for speed reasons.

In other words, as Petitioner persuasively argues, "[a]s to the 'why,' the Petition shows that (i) the POSITA would have been prompted to pursue a 'multiprocessor system' to facilitate 'parallel processing applications'; and (ii) the POSITA would have viewed Alexander's 'stacked FPGAs as preferable over alternatives' for achieving such a system." Reply 26 (quoting Pet. 60–61; Ex. 1002 ¶¶ 257–61). "And as to the 'how,' the Petition explains that 'the POSITA would have realized that using multiple FPGA dies in the stack as taught by Alexander would work in a straightforward manner similar manner to stacking multiple memories, or multiple microprocessors, as already taught in the Zavracky-Chiricescu- Akasaka Combination.'" *Id.* (quoting Pet. 60–61).

Patent Owner also alleges that the Petition fails to explain how to combine the references with a reasonable expectation of success. PO Resp. 55–57. Patent Owner alleges that "other sections of *Alexander* . . . [that] Petitioner wholly ignores . . . . do not suggest . . . that using multiple FPGA dies would work in a straightforward manner, let alone in Petitioner's proposed combination, so as to have a reasonable expectation of success." *Id.* at 56. Patent Owner provides little support for this argument. *See*

id. Contradicting Patent Owner, Alexander itself states that using multiple FPGAs in a stack results in a chip with "significantly smaller physical space," lower "power consumption," "shorter signal propagation delay," and "greater resource utilization and versatility" due to the "increased number of logic block neighbors" as "compared with a circuit-board-based 2D FPGA implementation." Ex. 1009, 253. In other words, Alexander suggests that stacked FPGAs implement the same circuitry of well-known single layer FPGAs, with numerous advantages.

Patent Owner also refers to sections in Alexander that describe thermal issues. PO Resp. 56. Patent Owner also argues that "Petitioner's threadbare argument that the combination is based on known methods to yield a predictable result (*see* Petition at 60–61) is . . . untethered to the features of the claimed invention." *Id.* at 57.

Contrary to these arguments, the Petition tethers the claimed stacking of two FPGAs to several reasons to combine the references. Patent Owner itself cites these reasons offered by Petitioner, including "offer[ing] FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor," and similarly "perform[ing] 'arbitrary logic functions,' . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in *Zavracky*," as noted above. *See* PO Resp. 55 (citing Pet. 19).

As Petitioner also argues, Patent Owner does not dispute that "Zavracky already taught combining an FPGA with a memory and microprocessor." Reply 27 (citing Ex. 1003, 12:29–39, Figure 13). Adding another FPGA layer in place of one of Zavracky's

microprocessors (Ex. 1003, Figs. 12, 13) therefore would have reduced thermal problems, "because FPGAs were more energy-efficient than microprocessors for the same size die, reducing heat." *Id.* (citing Ex. 1070 ¶¶ 37–41; Ex. 1058; Ex. 1082). Dr. Franzon's testimony includes an excerpt from DeHon (Ex. 1058) and Scrofano (Ex. 1082), which support Dr. Franzon's testimony that "FPGAs needed less power to get the same level of computing capability" as a processor. *See* Ex. 1070 ¶¶ 37–38 (citing Ex. 1058, 43). Similar to Alexander's teaching that "3D FPGAs have good implications with respect to power consumption" (Ex. 1009, 263), the '951 patent also evidences that 3D stacks "overall reduced power requirements" (Ex. 1001, 4:63). Reduced power translates to less heat, as was well-known and as Petitioner shows. *See infra* note 21.

Describing dual layer FPGA stacks, the '951 patent states as follows:

> It should be noted that although a single FPGA die 68 has been illustrated, *two or more FPGA die 68 may be included in the reconfigurable module 60. Through the use of the through- die area array contacts 70*, inter-cell connections *currently limited to two dimensions of a single die*, may be routed up and down the stack in three dimensions. *This is not known to be possible with any other currently available stacking techniques since they all require the stacking contacts to be located on the periphery of the die.* In this fashion, the number of FPGA die 68 cells that may be accessed within a specified time period is increased by up to 4 VT/3, where "V" is the

> propagation velocity of the wafer and "T" is the specified time of propagation.

Ex. 1001, 6:1–13 (emphasis added). Here, the '951 patent offers no description of any specific connection scheme between the two FPGA dies. It simply describes vias throughout the periphery of each die (instead of just at the periphery thereof) as a new technique (which is not correct), without any mention of heat problems associated with stacking two FPGAs. The '951 patent's lack of description and focus on vias throughout the whole die as a solution (providing speed gains) further evidences a reasonable expectation of success and supports Petitioner's showing.

As Petitioner also argues, thermal issues were a routine consideration, with known viable options to address the issues. Reply 27–28 (citing Ex. 1020, 11; Ex. 1070 ¶¶ 29–41; Ex. 1020; Ex. 1012; Ex. 1009; Ex. 1058; Ex. 1082). Dr. Franzon credibly lists known ways to dissipate heat, including use of low thermal resistance substrates, forced fluid coolants, thermal vias, and thermally conductive adhesives. Ex. 1070 ¶ 32.

The record also supports Dr. Franzon's testimony that "Alexander itself noted that thermal concerns were standard in any multi-chip design." *Id.* ¶ 36 (citing Ex. 1009, 256 (teaching that reducing power by eliminating I/O buffers, which Dr. Franzon states mitigates thermal issues (*see* Ex. 1070 ¶ 37 n.2)).[21] In

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[21] Testimony from footnote 2 of Dr. Franzon's declaration follows: "It would have been well known to the POSITA that in a chip, an increase in power usage generally translated to an increase in heat. For example, a processor using more power to perform

addition to mitigating heat concerns by eliminating I/O buffers (or "restrict[ing] I/O to one layer and plac[ing] it close to the heat sink," Ex. 1009, 256 § 5), in the same section, Alexander further supports Dr. Franzon's testimony, stating that "[a] number of . . . thermal-reduction techniques (i.e., thermal bumps and pillars . . ., thermal gels . . ., etc.) may also be applicable for 3D FPGAs." Ex. 1009, 255 § 5 ("Thermal Issues"). Alexander also states that "[a]s the power-to-area/volume ratio increases, so does the operating temperature unless heat can be effectively dissipated." *Id.*

As Petitioner also persuasively reasons, Patent Owner's arguments about heat dissipation concerns here do not undermine Petitioner's showing of a reasonable expectation of success, because a reasonable expectation of success "does not require a certainty of success." Reply 28 (quoting *Medichem v. Rolabo S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006)). As found above, Alexander promotes using multiple FPGAs in a module stack, and myriad additional evidence further supports a reasonable expectation of success. *See id.* (citing Ex. 1002 ¶¶ 44–45 (listing prior art showing FPGA stacks or FPGA stacks with microprocessors and memory), ¶¶ 260–261; Ex. 1009, 1).

Finally, none of the challenged claims, including claim 28, specifies the size of the claimed 3-D modules or FPGAs or a corresponding amount of computing power. Therefore, the breadth of claim 28 encompasses a 3-D stack operable on a minimal power

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computations will put off more heat than when the processor is using less power."

basis (and without any limit on the area of each element, further dissipating heat as the chip area increases), rendering heat concerns nonexistent or at least well within the bounds of a reasonable expectation of success. *See supra* note 21; Ex. 1009, 255–256 § 5 (discussed above, e.g., as power per unit area decreases, so does temperature).

We adopt and incorporate Petitioner's showing for claim 28, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14– 22, 58–61. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Alexander would have rendered obvious claim 28.

H. *Exhibit 1070*

Patent Owner argues that "[p]aragraphs 5–9, 13–28, 29–41, 44, 45, 59–66, 68, 73, 74, 76, 77, and 94–103 from Dr. Franzon's [Reply D]eclaration (Ex. 1070) addressing Petitioner's alleged obviousness grounds are not sufficiently discussed in the Reply" at pages 10, 13, 20, 21, 22, 25, and 27 of the Reply. Sur-reply 25. Patent Owner contends that the noted paragraphs are "not discussed in the Reply, but instead incorporated by citation or a cursorily parenthetical." *Id.* Patent Owner further contends that "the Board should not and cannot play archeologist with the record to search for the arguments" and "should not . . . consider[] Dr. Franzon's arguments." *Id.* (citing 37 C.F.R. § 42.6(a)(3) ("Arguments must not be

incorporated by reference from one document into another document.").

Patent Owner also cites *General Access Solutions, Ltd. v. Sprint Spectrum L.P.*, 811 F. App'x 654, 658 (Fed. Cir. 2020), as showing that the Board "cannot 'play[] archaeologist with the record." Sur-Reply 25. The situation here is different than in *Sprint Spectrum*, because there, the court noted a problem with identifying a party's substantive arguments *prior to turning to the declaration at issue*: "*To identify GAS's substantive arguments*, the Board was forced to turn to a declaration by Struhsaker, *and further to delve into a twenty-nine-page claim chart attached as an exhibit*." *Id.* (emphasis added).

Here, Patent Owner does not describe or allege any problem with identifying Petitioner's substantive arguments. In context, except as discussed below, the cited paragraphs of Dr. Franzon's Reply Declaration (Ex. 1070) properly support Petitioner's substantive arguments at the pages of the Reply identified by Patent Owner.

Regarding the first citation, page 10 of the Reply cites paragraphs 94–103 of Dr. Franzon's Reply Declaration, and discusses how, even if the "functional to accelerate" clauses require "a wide configuration data port," the combination of Zavracky, Chiricescu, and Akasaka teaches it. *See* Reply 9–10 (citing Ex. 1070 ¶¶ 94–103). This citation is a misprint or oversight by Petitioner, because Dr. Franzon's Reply Declaration does not include paragraphs 96–102. Therefore, any issue with respect to those paragraphs is moot. The remaining cited paragraphs of Dr. Franzon's Reply Declaration on page 10 of the Reply directly relate to what a "wide

configuration data port" constitutes. Also, paragraph 95 reproduces some of the same testimony by Dr. Chakrabarty (Patent Owner's expert in IPR2020-01021) that the Reply discusses and reproduces on page 10 of the Reply.

Regarding the second citation, page 13 of the Reply cites two paragraphs with a parenthetical as follows: "Ex. 1070¶¶73–74 (citing Ex. 1083, an example of common usage of 'share data' as 'transfer data')." Prior to the citation, the Reply addresses the plain meaning of "share," tracking the parenthetical. *See* Reply 13. Notwithstanding that Patent Owner generally implies that citation is one of several examples of "a cursorily parenthetical" (Sur-reply 25), the parenthetical is clear as to how Dr. Franzon's cited testimony supports Petitioner's Reply argument.

Regarding the third citation, page 19 of the Reply (citing Ex. 1070 ¶¶ 13–28), Petitioner's argument merely responds to a summary argument by Patent Owner about four different "TSV interconnection issues." *See* PO Resp. 41 ("At the time of the invention, a POSITA was aware of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ('HDL') algorithms, which must be considered." (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89); Reply 19 ("The supposed 'TSV interconnection issues' that [Patent Owner] cursorily identifies were at most normal engineering issues, not problems preventing a combination. Ex. 1070 ¶¶ 13–28 (Dr. Franzon rebutting Dr. Souri's testimony as to every purported issue with citations to evidence)." Here, Petitioner's parenthetical generally informs the reader that Dr. Franzon's testimony responds to Dr.

Souri's "cursor[y]" summary alleging "TSV interconnection issues." *See* Reply 20; PO Resp. 41.

Paragraphs 13–20 of Dr. Franzon's Reply Declaration provide background context leading to thrust of paragraphs 21–28, which directly support Petitioner's Reply argument that TSV issues were normal engineering issues in the context of combining the references. Therefore, we consider cited paragraphs 13–20 only as background information and context.

In comparison, providing his testimony about the TSV issues, Dr. Souri's support for TSV issues is a citation to "Ex. 2014 at 85, 97, 90." Ex. 2011 ¶ 82. Patent Owner provides the same citation without any explanation of the citation. PO Resp. 41. This amounts to the same type of incorporation-by-reference of pages of evidence that Patent Owner attributes to Petitioner. Also, the cited three pages of Exhibit 2014 are in the middle of an industry article, and the pages are densely packed two-column pages that facially appear to have at least the same number of words in some of the complained-about citations to multiple paragraphs that Petitioner provides to Dr. Souri's Reply Declaration. Here, Patent Owner leaves it to the Board to dig into the cited pages of Exhibit 2014 to find the alleged TSV interconnection issues and place it in context to the background information in the whole article. In reaching our decision, we exercised judgment as to all the evidence cited by the parties for its relevance, context, and substance, and weighed it accordingly.

Finally, an examination of the other citations identified by Patent Owner in full context, reveals (like the citations addressed above) that Petitioner's

use of and citation to Dr. Souri's testimony is not improper. In summary, the remaining pages of the Reply identified by Patent Owner include citations with a clear sentence preceding the citation and/or clear parenthetical informing the reader clearly how the cited testimony supports the sentence. *See* Reply 21 n.8 (clear parenthetical and preceding sentence) (citing Ex. 1070 ¶¶ 59–66), 22 (clear preceding sentence (citing Ex. 1070 ¶¶ 44–45)), 25 (clear preceding sentence (citing Ex. 1070 ¶¶ 76–77)), 27 (clear parentheticals and preceding sentences (citing Ex. 1070 ¶¶ 37–41 and Ex. 1070 ¶¶ 29–41)).

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.[22] In summary:

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent-able
1, 2, 4–6, 8–24, 27, 29	103(a)	Zavracky, Chiricescu, Akasaka	1, 2, 4–6, 8–24, 27, 29	

[22] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent-able
25	103(a)	Zavracky, Chiricescu, Akasaka, Trimberger	25	
26		Zavracky, Chiricescu, Akasaka, Satoh	26	
28		Zavracky, Chiricescu, Akasaka, Alexander	28	
Overall Outcome			1, 2, 4–6, 8–29	

IV. ORDER

Accordingly, it is

In consideration of the foregoing, it is hereby

ORDERED that claims 1, 2, 4–6, and 8–29 of the '951 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

APPENDIX F

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case IPR2020-01570[1]
Patent RE42,035 E

XILINX, INC., PETITIONER,

v.

ARBOR GLOBAL STRATEGIES, LLC, PATENT OWNER

Entered: Mar. 2, 2022

FINAL WRITTEN DECISION

35 U.S.C. § 318(a)

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, Administrative Patent Judge.

Xilinx, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–38 (the "challenged claims") of U.S. Patent No. RE42,035 B2 (Ex. 1001, the "'035 patent"). Pet. 1.

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[1] Taiwan Semiconductor Manufacturing Co. Ltd. ("TSMC") filed a petition in IPR2021-00737, and the Board joined it as a party to this proceeding. *See also* Paper 39 (order dismissing-in-part TSMC as a party with respect to claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29).

Petitioner filed a Declaration of Dr. Paul Franzon (Ex. 1002) with its Petition. Arbor Global Strategies LLC ("Patent Owner") filed a Preliminary Response (Paper 8, "Prelim. Resp.").

After the Institution Decision (Paper 13, "Inst. Dec."), Patent Owner filed a Patent Owner Response (Paper 19, "PO Resp.") and a Declaration of Dr. Shukri J. Souri (Ex. 2011); Petitioner filed a Reply (Paper 23) and a Reply Declaration of Dr. Paul Franzon (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 27). Thereafter, the parties presented oral arguments via a video hearing (Dec. 3, 2021), and the Board entered a transcript into the record. Paper 33 ("Tr.").

For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

Petitioner identifies Xilinx, Inc. as the real party-in-interest. Pet. 72. Patent Owner identifies Arbor Global Strategies LLC. Paper 5, 1. Joined party Taiwan Semiconductor Manufacturing Co. Ltd. is also a real party-in- interest. *See supra* note 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC, v. Xilinx, Inc.*, No. 19-CV-1986-MN (D. Del.) (filed Oct. 18, 2019) as a related infringement action involving the '035 patent and three related patents, U.S. Patent No. 7,282,951 B2 (the "'951 patent"), U.S. Patent No. 6,781,226 B2 (the "'226 patent") and U.S. Patent No. 7,126,214 B2 (the "'214 patent"). *See* Pet. 72–73; Paper

5. Petitioner "contemporaneously fil[ed] *inter partes* review (IPR)] petitions challenging claims in each of these patents," namely IPR2020-01567 (challenging the '214 patent), IPR2020-01568 (challenging the '951 patent), and IPR2020-01571 (challenging the '226 patent). *See* Pet. 72. Final written decisions for these three cases issue concurrently with the instant Final Written Decision.

The parties also identify *Arbor Global Strategies LLC* v. *Samsung Electronics Co., Ltd.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) as a related infringement action involving the '035, '951, and '226 patents. Subsequent to the complaint in this district court case, Samsung Electronics Co., Ltd. ("Samsung") filed petitions challenging the three patents, and the Board instituted on all challenged claims, in IPR2020- 01020, IPR2020-01021, and IPR2020-01022. *See* IPR2020-01020, Paper 11 (decision instituting on claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the '035 patent); IPR2020-01021, Paper 11 (decision instituting on claims 1, 4, 5, 8, 10, and 13–15 the '951 patent); IPR2020-01022, Paper 12 (decision instituting on claims 13, 14, 16–23, and 25–30 of the '226 patent).

The Board recently issued final written decisions in the three Samsung cases, determining all challenged claims unpatentable. *See* IPR2020-01020, Paper 30 (holding unpatentable claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29 of the '035 patent); IPR2020-01021, Paper 30 (holding unpatentable claims 1, 4, 5, 8, 10, and 13–15 of the '951 patent); IPR2020-01022, Paper 34 (holding unpatentable claims 13, 14, 16–23, and 25–30 of the '226 patent). The Board joined Taiwan Semiconductor

Manufacturing Co. Ltd. as a party in each of the prior proceedings as it did here.

C. *The '035 patent*

The '035 patent describes a stack of integrated circuit ("IC") die elements including a field programmable gate array ("FPGA") on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '035 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." *Id.*

Figure 4 follows:

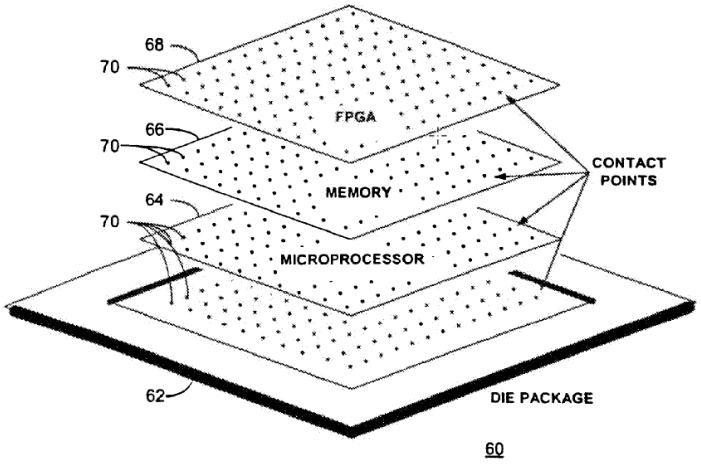

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64,

interconnected using contact holes 70. Ex. 1001, 4:6–20.

The '035 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:17–32. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See id.* Such a "reconfigurable processor" also provides a known benefit of flexibly providing different types of different logical units required by an application after manufacture or initial use. *See id.*

D. *Illustrative Claims 1 and 23*

Independent claims 1 and 23 illustrate the challenged claims at issue:

> 1. A processor module comprising:
>
> [1.1] at least a first integrated circuit die element including a programmable array;
>
> [1.2] at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and
>
> [1.3] wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and
>
> [1.4] wherein said contact points traverse said die elements through a thickness thereof.

Ex. 1001, 6:11–22.

23. A programmable array module comprising:

[23.1] at least a first integrated circuit die element including a field programmable gate array;

[23.2] at least a second integrated circuit die element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit die element; and

[23.3] wherein said field programmable gate array is programmable as a processing element, and

[23.4] wherein said memory array is functional to accelerate external memory references to said processing element.

Ex. 1001, 7:38.

E. *The Asserted Grounds*

Petitioner challenges claims 1–38 of the '035 patent as follows (Pet. 1):

Claims Challenged	35 U.S.C. §	References
1–30, 33, 36, 38	103[2]	Zavracky,[3] Chiricescu,[4] Akasaka[5]
31, 32, 34	103	Zavracky, Chiricescu, Akasaka,

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of trial, the '035 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

[3] Zavracky et al., US 5,656,548, issued Aug. 12, 1997. Ex. 1003.

[4] Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98. Ex. 1004.

[5] Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Iss. 12, pp. 1703-1714, Dec. 1986, ISSN 0018-9219. Ex. 1005.

Claims Challenged	35 U.S.C. §	References
		Trimberger[6]
35	103	Zavracky, Chiricescu, Akasaka, Satoh[7]
37	103	Zavracky, Chiricescu, Akasaka, Alexander[8]

II. ANALYSIS

A. *Legal Standards*

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art;

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[6] Steve Trimberger et al., *A Time-Multiplexed FPGA*, Proceedings of the 1997 IEEE International Symposium on Field-Programmable Custom Computing Machines, April 1997, ISBN 0-8186-8159-4.

[7] Satoh, PCT App. Pub. No. WO00/62339, published Oct. 19, 2000. Ex. 1008 (English translation).

[8] Michael J. Alexander, James P. Cohoon, Jared L. Colflesh, John Karro, and Gabriel Robins, *Three-Dimensional Field-Programmable Gate Arrays*, Proceedings of Eighth International Application Specific Integrated Circuits Conference, Sept. 1995. Ex. 1009.

(3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. *Level of Ordinary Skill in the Art*

Relying on the testimony of Dr. Franzon, Petitioner contends that

> [t]he person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '035 patent would have been a person with a Bachelor's Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication.

Pet. 7 (citing Ex. 1002 ¶¶ 58–60).

Relying on the testimony of Dr. Souri, Patent Owner contends that

> [a] person of ordinary skill in the art ("POSITA") around December 5, 2001 (the earliest effective filing date of the '035 Patent) would have had a Bachelor's degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.

PO Resp. 8–9 (citing Ex. 2011 ¶ 25).

We adopt Petitioner's proposed level of ordinary skill in the art as we did in the Institution Decision, because it comports with the teachings of the '035 patent and the asserted prior art. *See* Inst. Dec. 20–

21. Patent Owner's proposed level largely overlaps with Petitioner's proposed level. Even if we adopted Patent Owner's proposed level, the outcome would not change.

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b) (2020). Under this standard, which is the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

In the Institution Decision, we determined that

> [t]he parties' arguments raise a claim construction issue regarding "wherein said memory array is functional to accelerate external memory references to said processing element" (claims 23 and 33) and "said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory array is functional to accelerate reconfiguration of said field

> programmable gate array as a processing element" (claims 24, 30, and 32). Neither party provides an explicit construction.

Inst. Dec. 21–22. Tracking the institution decision in related IPR2020- 01021 (challenging related U.S. Patent No. 7,282,951 B2), in the Institution Decision here, we preliminarily construed the "'functional to accelerate' limitations [as] requir[ing] a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and processor." Inst. Dec. 25.[9] Likewise, in the final written decision in IPR2020-01021 and in co-pending IPR2020-01568, the Board construed these "functional to accelerate" limitations in materially the same manner. IPR2020-01021, Paper 30, 26, Paper 33 (Errata); IPR2020-01568, Paper 39 (final written decision) § II.C.

In particular, the "functional to accelerate" clauses require "a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array." *See* IPR2020-01021,

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[9] The two relevant patent specifications (i.e., for U.S. Patent No. 7,282,951 B2 and the '035 patent) include the same material disclosure for claim construction purposes. The application leading to U.S. Patent No. 7,282,951 B2 is a continuation of an application leading to US. Pat. No. 7,126,214 B2, which is a continuation-in-part an application leading to U.S. Pat. No. 6,781,226 B1, which is a continuation-in-part of the application leading to U.S. Patent No. 6,627,985 B2, from which the '035 patent reissued. *See* Ex. 1001, codes (21), (64); IPR20-01021, Ex. 1001, codes (21), (63).

Paper 30, 26, Paper 33 (Errata). We herein adopt and incorporate the construction and the rationale supporting it from the final written decision of IPR2020-01021.

Petitioner states that "[e]ven beyond the Board's construction, the Petition shows that the Zavracky-Chiricescu-Akasaka Combination provides the 'memory array . . . accelerate' limitations under ***any*** reasonable construction," "even under [Patent Owner's] flawed construction." Reply 8–9. Patent Owner states that it "construes all terms in 'accordance with the ordinary and customary meaning of such claim as understood by on of ordinary skill in the art and the prosecution history pertaining to the patent.'" PO Resp. 9 (quoting 37 C.F.R. § 42.100(b)).

Patent Owner argues that "the claims require . . . structure provided ***within the memory array*** (i.e. the wide configuration data port disclosed in the '035 Patent) that is responsible for accelerating the programmable array's accelerated external memory references." PO Resp. 20 (citing Ex. 2011 ¶ 55). Contrary to this argument, Patent Owner fails to describe what particular structure of a wide configuration data port (WCDP) within a memory array the challenged claims require under "the ordinary and customary meaning" or otherwise. *See id.* at 9. The '035 patent does not describe a WCDP "within the memory array." Figure 5, for example, depicts "VERY WIDE CONFIGURATION DATA PORT" 82, but Figure 5's WCDP is a separate black box from any structure involving memory or a memory array. *Compare* Ex. 1001, Fig. 4 (memory die 66 and vias 70), *with id.* at Fig. 5 (WCDP 82).

Figure 5 follows:

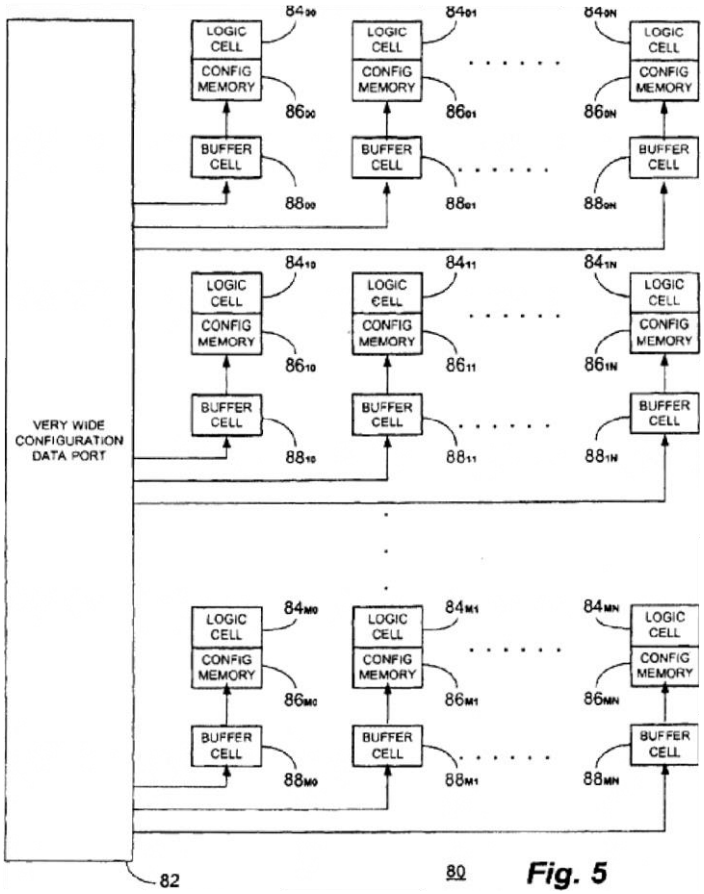

Fig. 5

Figure 5 above illustrates a "VERY" WCDP 82 on the left connected to buffer cells 88, and configuration memory cells 88 and logic cells 84, toward the middle and right of the WCDP. *See* Ex. 1001, Fig. 5; 4:50–56. Buffer cells 88 ("preferably on a portion of the memory die 66" (*see* Fig. 4)), "can be loaded while the FPGA 68

comprising the logic cells 84 *are* [sic] *in operation*." *Id.* at 4:51–53 (emphasis added).[10]

Therefore, the central purpose of the buffer cells is "*they can be loaded while the FPGA 68 comprising the logic cells are in operation*," which "then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it[s] configuration cells 84 updated in parallel." *Id.* at 4:53– 53 (emphasis added). But none of the challenged claims require loading the FPGA while it is in operation. Also, configuration cells and the FPGA can be updated in parallel (e.g., in one clock cycle) without the buffer cells. *See id.*; *see also infra*

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[10] Although the '035 patent states that "[t]he buffer cells 88 are preferably on a portion of the memory die 66 (FIG. 4)" in reference to Figure 5, the buffer cells 88 in Figure 5 appear to be near or connected to FPGA logic cells 84 and configuration memory cells 86—perhaps depicting something other than the preferred embodiment describing buffer cells on the memory die. For example, Dr. Chakrabarty (Patent Owner's expert in related IPR1020-01021) testified that FPGA die 68 is to the right of Figure 5's WCDP 82, while memory die 66 (*see* Fig. 4), although undepicted in Figure 5, is to the left of Figure 5's WCDP 82. Ex. 1075, 157:5–158:7; *see also* Reply 9 (quoting 1075, 157:23–158:3). In any event, Figure 5 depicts WCDP 82 as a separate circuit or structure (in black box form) from buffer cells 88 and any memory die or array, and it is not clear how Figure 5's WCDP relates structurally to a memory die or memory array. *See id.* at Fig. 5.

During the Oral Hearing, Patent Owner's arguments further blurred what Figure 5 illustrates. That is, Patent Owner argued that "when the buffer cells are on the FPGA, it then raises the question, okay, well, what's on the memory array, right. And my answer would be *probably* more buffer cells." Tr. 54:21–24 (emphasis added). But there is no disclosure for buffer cells in or on both a memory array and an FPGA die. *See id.* at 55:3–6 (Patent Owner arguing that "I don't think there's anything *that prevents*" buffer cells from being on both dies (emphasis added)).

note 11 (cache memory provides reconfiguration). Therefore, the claims do not require buffer cells even by implication.

Regardless of the location of the disclosed but unclaimed buffer cells, Figures 4 and 5 and the disclosure indicate that the numerous connections between memory die 66 (with or without buffer cells 88 thereon) and FPGA die 68 (with our without configuration memory cells 86 thereon) facilitate the claimed "functional to accelerate" limitations, in line with our claim construction.[11] In other words, to the extent the claims implicate a WCDP, it is the numerous via connections associated with that port connected to a memory or memory array that support the "functional to accelerate" limitations as discussed further below.

Patent Owner correctly notes that "the '035 Patent discloses that loading configuration data through a typical, relatively narrow [i.e., '8 bit' or single 'byte'] configuration data port [with respect to prior art Figure 3] led to unacceptably long reconfiguration times." *See* PO Resp. 20 (citing Ex. 1001, 3:66–4:5); Ex. 1001, 3:66–4:5 ("Configuration data is loaded through a configuration data port in a *byte serial* fashion and must configure the cells

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[11] The '035 patent implies that configuration memory cells 66 are on FPGA die 68 in one embodiment, but a cache memory provides reconfiguration without them in other embodiments. *See* Ex. 1001, 4:56–61 (stating that "[o]ther methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory ('RAM') than can be offered within the FPGA die itself").

sequentially progressing through the entire array of logic cells 54 and associated configuration memory. It is the loading of this data through a relatively narrow, for example, *8 bit port* that results in the long reconfiguration times." (emphasis added)).[12] Patent Owner contends that "[t]he inventors solved this problem not only by stacking a memory die with a programmable array die, but also *by interconnecting those two elements* with a 'wide configuration data port' that employs through-silicon contacts, with the potential for even further acceleration where the memory die is 'tri- ported.'" *Id.* (citing Ex. 1001, 4:31–38) (emphasis added). This argument itself (which mimics the testimony of Dr. Souri (Ex. 2011 ¶ 56)) shows that any structure of a WCDP implicated here simply "interconnect[s] those two [die] elements"—i.e., implicating the numerous vias/contacts 70 as depicted in Figure 4 that connect die elements 64, 66, and 68 together. Therefore, Patent Owner's argument and Dr. Souri's testimony support our analysis and claim construction.

In another argument addressing Petitioner's allegation of obviousness, Patent Owner argues that Petitioner "does not account for all aspects of the

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[12] This description indicates that 8 bits of the single byte load in parallel to the first 8 bit locations of configuration memory 56, and then in succession (serial) to the other configuration memory cells. In other words, the quoted description about "byte serial" loading and Figure 3 together show that each byte (i.e., 8 bits) loads over a parallel bus into successive 8 bit blocks (i.e., a byte) of configuration memory cells in succession (i.e., series). *See* Ex. 1001, Fig. 3 (showing 8 bit configuration data port 52 connected by a bus to a block of configuration memory cells 56_{M0} and then in serial to successive blocks of configuration memory cells 56_{M1}–56_{00}).

claimed invention," and states "[f]or example, . . . the '035 patent . . . discloses utilizing a portion of the memory array as a wide configuration data port including buffer cells." PO Resp. 22 (citing Ex. 1001, 4:47–52). Note that this argument for "buffer cells" differs from Patent Owner's argument on page 20 of its Response, which does not mention "buffer cells" and only mentions a "wide configuration data port" as "responsible for accelerating the programmable array's accelerated external memory references." Again, the argument does not explain how the '951 patent shows "utilizing a portion of the memory array as a wide configuration data port."

Based on the specification and claim language as discussed above and further below, apart from numerous vias 70 as depicted in Figure 4, none of the "functional to accelerate" clauses at issue here require any other structure associated with a WCDP.

In support of our claim construction, Figure 4 of the '035 patent, depicted next, illustrates vias 70 throughout each die, 64, 66, and 68:

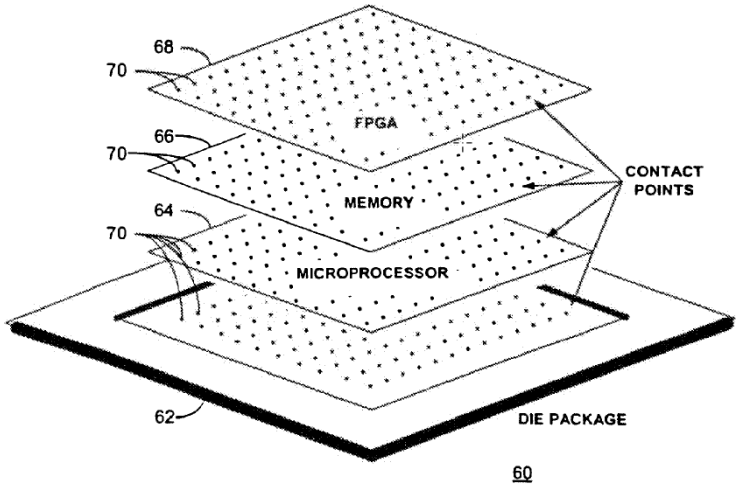

Fig. 4

As depicted above, Figure 4 shows a number of vias 70 throughout the periphery of each die (i.e., microprocessor die 64, memory die 66, and FPGA 68 die). According to the abstract as quoted above, these "contacts [i.e., vias] . . . traverse the thickness of the die. The processor module disclosed allows for a *significant acceleration* in the sharing of data between the microprocessor and the FPGA element . . . ." Ex. 1001, code (57) (emphasis added). This description of "*significant acceleration*" does not mention a WCDP or buffer cells.

Moreover, the '035 patent specification consistently ties data acceleration to stacking techniques that include vias throughout the stacked dies without requiring other structure. In addition to the abstract, the '035 patent describes "taking advantage of the significantly increased number of

connections to the cache memory die." Ex. 1001, 4:56–58. It describes "an FPGA module that uses *stacking techniques* to combine it with a memory die *for the purpose of accelerating* FPGA *reconfiguration*." *Id.* at 2:55–57 (emphasis added). Similarly, it states that "the FPGA module may employ *stacking techniques* to combine it with a memory die *for the purpose of accelerating external memory references*." *Id.* at 2:59–60 (emphasis added). The stacking techniques include and refer to the short multiple through-via interconnections 70 *distributed throughout the dies* as depicted in Figure 4. *Id.* at 2:31–35 ("[S]ince these differing die do not require wire bonding to interconnect, it is now also possible to place interconnect pads throughout the total area of the various die rather than just around their periphery. This allows for many more connections between the die than could be achieved with any other known technique.").

The '035 patent also explains that "[b]ecause the various die 64, 66 and 68 (FIG. 4) have *very short electrical paths* between them, the signal levels can be reduced while at the same time *the interconnect clock speeds can be increased*." Ex. 1001, 4:64–66 (emphasis added). Similarly, "there is an added benefit of . . . *increased operational bandwidth*." *Id.* at 4:62–63 (emphasis added). As summarized here, these descriptions of shorter electrical paths, increased speed and bandwidth (leading to data acceleration), and acceleration in general, all because of the disclosed stacking techniques (which include multiple short through-vias), apply generally to such speed increases (i.e., acceleration) in the context of Figure 4 without mention of Figure 5's WCDP and buffer cell embodiment, or any tri-port structure. As noted

above, even reconfiguration may occur without the specific black box WCDP embodiment of Figure 5, for example, "[o]ther methods for taking advantage of *the significantly increased number of connections* to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68." *Id.* at 4:56–61 (emphasis added); *see supra* note 11.

Based on the arguments and evidence of record, no reason exists to depart from the claim construction set forth in the final written decision IPR2020-01021. As Petitioner also argues, Patent Owner did not assert a clear requirement for a WCDP and/or buffer cells for the "functional to accelerate" in related district court litigation. *See* Reply 2–3 (arguing that Patent Owner does not justify incorporating limitations from the specification and "has taken five inconsistent positions on the 'accelerate' terms across co-pending IPRs and litigations") (citing Ex. 1071 (district court claim chart)); Ex. 1071 (listing various claim construction statements by Patent Owner); Ex. 1072, 27).

For example, in the district court litigation, Patent Owner argued as follows:

> The specification teaches *in several sections* that *the short interconnects to the memory die allows for accelerated external memory references*, providing additional context for a POSITA to interpret the claims. Darveaux Decl., ¶ 35. For example, the '951 Patent states that in reference to Figures 4 and 5 that *acceleration* to external memory *is performed because "the FPGA module may employ stacking techniques to combine it with a memory die for accelerating external*

> *memory references as well as to expand its on chip block memory*." Ex. 2, '951 Patent at Figs. 4 and 5, 2:56-3:2 (emphasis added).

Ex. 1072, 29 (emphasis added).

In other words, this passage shows that Patent Owner argued in the district court that "short interconnects" of the disclosed "stacking techniques" improve the speed relative to the prior art—without relying specifically on a WCDP, buffer cells, or parallel processing. *See id.* Therefore, contrary to arguments in the Sur-reply, even though Patent Owner advanced other arguments during the district court litigation, none are clear enough to overcome Patent Owner's broad statements in the district court litigation as quoted above, and Patent Owner has not "taken consistent positions across all IPRs and litigations." *See* Sur-reply 2.

As the Board also preliminarily determined in the Institution Decision, prosecution history of the related '951 patent application also plays an important role in understanding the claims and supports the preliminary claim construction. *See* Inst. Dec. 24; *accord* Ex. 2009 (institution decision in IPR2020-1021), 24–25. The prosecution history of the '951 patent application further supports our construction of the materially similar accelerate clauses involved in the '951 patent claims and the '035 patent claims.

Specifically, the Examiner indicated allowance of dependent claim 35 of the '951 patent (if written in independent form) over Lin (U.S. Patent No. 6,451,626 B1 (Ex. 1054; Ex. 1107, 67)), finding Lin does not teach or suggest "wherein said memory

array is functional to accelerate external memory references to said processing element." Ex. 1107, 72– 73; Inst. Dec. 24–25.

Noting this in our Institution Decision, we pointed to petitioner Samsung's annotation in the IPR1020-01021 proceeding of the following figures from Lin to illustrate the issue:

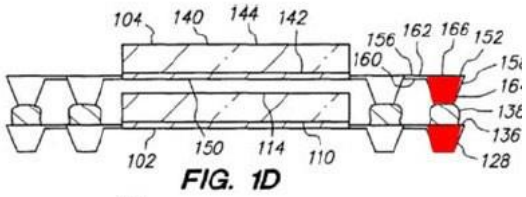

FIG. 1D

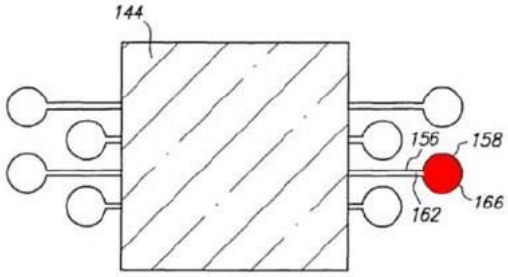

FIG. 2D

Ex. 2009, 25; Inst. Dec. 25. Lin's annotated Figures 1D and 2D above show that Lin discloses contacts (red) on the sides of dies, instead of a number contact vias extending throughout the area of each die within the periphery thereof, in line with the Examiner's reasons for allowance. *See id.*; Ex. 1054 (Lin), Figs. 1D, 2D; Ex. 1107, 72–73.

Accordingly, as we noted in the Institution Decision,

> in light of Lin's teachings and absent explicit explanation during prosecution by the Examiner, the rejection and reasons for

> allowance provide further support the understanding that the "functional to accelerate" limitations require a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and process[ing element].

Inst. Dec. 25–26; *compare*, Ex. 1001, Fig. 4 (showing numerous contact points), *with* Ex. 1054, Figs. 1D, 2D (showing peripheral contact points).

During the Oral Hearing, Patent Owner argued that with respect to a WCDP that *"[t]he spec is very clear that what we're talking about is it has enough connections to allow the parallel updating of data*." Tr. 48:20–22 (emphasis added). When asked to compare the '035 patent's Figure 3 (which depicts a prior art eight bit configuration data port) and Figure 5 (which depicts a WCDP), Patent Owner stated that the WCDP "could be as small as 32 bits . . . if you have a small FPGA, right? If you want to update something in parallel, you could update 32-bit with 32 bits?" Tr. 49:1–9 (answering "yes, . . . if you have a very, . . . small FPGA, the number of bits can be . . . relatively smaller, but what's critical is not the number of bits and . . . . [i]t's not necessarily the number of bits that's in the configuration data port, but how they're arranged"). Patent Owner continued by answering that "parallel connections between cells on the die. . . . get to the heart of what the wide configuration data port is, how it works, and how the interconnections between the die work even absent . . . the data being used to configure the FPGA." *Id.* at 49:13–16. Then, Patent Owner argued that "*we all agree* that the wide

configuration data port . . . *at least includes these interconnections between the die*. So, what we're talking about is *moving data from one die to another*. *That's the use of the wide configuration data port*." *Id.* at 49:22–50:4 (emphasis added).

These arguments support our construction because our construction "at least includes these interconnections between the die" and allows data movement between dies. In addition, contrary to Patent Owner's arguments in the Sur-reply, our construction implicitly distinguishes over the small number of connections in the narrow configuration data port of the '035 patent's prior art Figure 3. *See* Sur-reply 8 (arguing that "Petitioner's . . . interpretation of the wide configuration data port as simply meaning 'a data port used for configuration . . . . [with] a lot of connections though these TSVs' [through silicon vias] . . . . directly contradict[s] the specification [and] . . . also encompasses the conventional 'data port,' which the '035 Patent distinguishes the wide configuration data port from" (quoting Reply 8).

In other words, the "functional to accelerate" clauses require "a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory array and processing element." *See* IPR2020-01021, Paper 30, 26, Paper 33 (Errata). This implicitly represents more vias than prior art Figure 3 of the '035 patent describes (i.e., eight), as supported in view of specification and the prosecution history of the related '951 patent. *See* Ex. 1001, Fig. 3 ("8 BIT

CONFIGURATION DATA PORT 52"). In addition, as discussed further below and as Petitioner shows, to the extent any of the "functional to accelerate" claims implicate parallel data transfer, our claim construction *allows for* such parallel data transfers—in line with Patent Owner's arguments. *See* Tr. 49:13–16 (Patent Owner arguing that "parallel connections between cells on the die. . . . get to the heart of what the wide configuration data port is, how it works, and how the interconnections between the die work"); Sur-reply 2 (arguing that "the novel die-area interconnection arrangement with buffer cells (i.e., wide configuration data port) *allows the parallel loading of data* from the memory die to the programmable array that is responsible for the claimed acceleration" (emphasis added)).

Moreover, Patent Owner concedes that "[t]he '035 Patent makes clear that stacking die and short interconnections are simply 'added benefits' that allow for *increased operational bandwidth and speed*." Sur-reply 6 (citing Ex. 1001, 4:62–67) (emphasis added). But increased speed is acceleration—not merely "an added benefit." So is increased bandwidth in context to the '035 patent, because both benefits of *increase in speed* and bandwidth fall within the "functional to accelerate" limitations at issue here for the reasons discussed above. *See* Ex. 1001, 4:42–66; Tr. 56:11–14 (Patent Owner arguing that "[i]f you have a data port that connects in parallel the cells in the memory array with the FPGA cells, that does massively increase bandwidth. . . . but just increasing bandwidth doesn't get you parallel connections"). As noted, our claim construction allows for parallel data transfers (i.e., "a number of vertical contacts distributed

throughout . . . to allow multiple short paths for data transfer") so that an increase in bandwidth due to such multiple data paths (vias and connections) both satisfies and supports the "functional to accelerate" clauses.

Therefore, as indicated above, we construe the "functional to accelerate" limitations as "a number of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the "memory array/memory and processing element/programmable array."

Based on the current record, no other terms require explicit construction. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'. . . ." (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness, Claims 1–30, 33, 36, and 38*

Petitioner contends the subject matter of claims 1–30, 33, 36, and 38 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 13–55. As discussed below, Patent Owner disputes Petitioner's contentions. *See generally* PO Resp.; Sur-reply.

1. *Zavracky*

Zavracky, titled "Method for Forming Three Dimensional processor Using Transferred Thin Film Circuits," describes "[a] multi-layered structure" including a "microprocessor . . . configured in different

layers and interconnected vertically through insulating layers which separate each circuit layer of the structure." Ex. 1003, code (57). Zavracky's "invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing." *Id.* at 2:5–10. Zavracky includes numerous types of stacked elements, including "programmable logic device[s]" stacked with "memory" and "microprocessor[s]." *See id.* at 5:19–23.

Zavracky's Figure 12 follows:

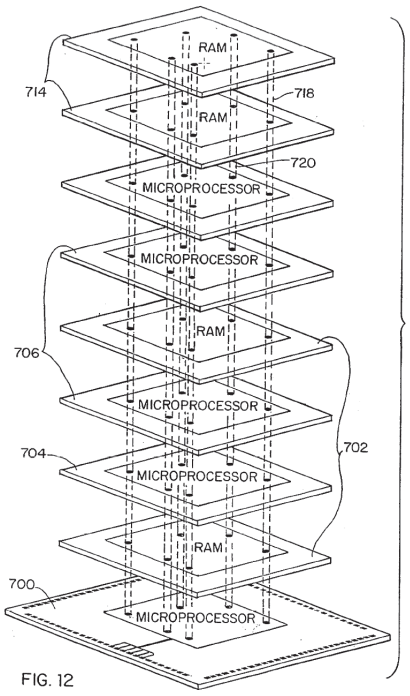

FIG. 12

Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements wherein "buses run

vertically through the stack by the use of inter-layer connectors." Ex. 1003, 12:24–26.

2. *Chiricescu*

Chiricescu, titled "A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data," describes a three- dimensional chip, comprising an FPGA, memory, and routing layers. Ex. 1004, II-232. Chiricescu's FPGA includes a "layer of on-chip random access memory . . . to store configuration information." *Id.* at II-232 § 1. Chiricescu describes and cites the published patent application that corresponds to Zavracky (Ex. 1003) as follows:

> At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits *and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip*.

See id. at II-232; *see also id.* at II-235 (citing "P. Zavracky, M. Zavracky, D- P Vu and B. Dingle, '*Three Dimensional Processor using Transferred Thin Film Circuits*,' US Patent Application # 08-531-177, allowed January 8, 1997") (emphasis added).[13]

Chiricescu describes "[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information." Ex. 1004, II-232 § 1. Chiricescu also describes using

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[13] Zavracky lists the same four inventors and "Appl. No. 531,177," which corresponds to the application number cited by Chiricescu. Ex. 1003, codes (75), (21).

memory on-chip to "significantly improve[] the reconfiguration time," explaining as follows:

> The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to manage cache memory can be used to administer the configuration data.

Id. at II-234.

Figure 2 of Chiricescu follows:

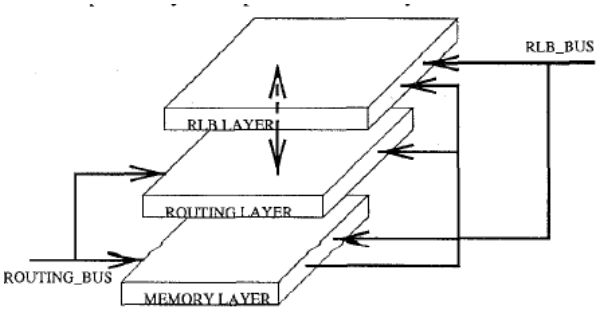

Figure 2. The layers of our 3-D FPGA architecture.

Chiricescu's Figure 2 above illustrates three layers in the 3-D-FPGA architecture, with a "routing and logic blocks" (RLB) layer arranged in a "sea-of-gates FPGA structure," a routing layer, and the aforementioned memory layer (to program/reconfigure the FPGA). *See* Ex. 1004, II-232–233. "[E]ach RLB is connected with the switch-boxes . . . in the routing layer (RL) by means of inter-layer vias. Each RLB can be configured to implement a D-type register and an arbitrary logic function of up to three variables." *Id.* at II-232. Figure 2 also depicts an external "ROUTING_BUS" to access the 3-D

structure with external circuitry to provide configuration data. *Id.* at II-232 ("A routing bus provides the configuration information of the routing layer . . . .").

3. *Akasaka*

Akasaka, titled "Three-Dimensional IC Trends" (1986), generally describes trends (several years before the 2001 effective filing date of the invention) in three-dimensional integrated stacked active layers. Ex. 1005, 1703. Akasaka states that "tens of thousands of via holes" allow for parallel processing in stacked 3-D chips, and the "via holes in 3-D ICs" decrease the interconnection length between IC die elements so that "the signal processing speed of the system will be greatly improved." *Id.* at 1705. Akasaka further explains that "[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing" so that "twice the operating speed is possible in the best case of 3-D ICs." *Id.*

Also, "input and output circuits . . . consume high electrical power." Ex. 1005, 1705. However, "a 10-layer 3-D IC needs only one set of I/O circuits," so "power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs." *Id.*

Figure 4 of Akasaka follows:

Fig. 4. Wiring for parallel processing in 2-D and 3-D ICs.

Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

According to Akasaka, "[p]arallel processing is expected to be realized more easily in 3-D structures. Several thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or *vice versa*) through them." Ex. 1005, 1705. As one example, Akasaka describes one 3-D chip as including "a video sensor on the top layer, then an A/D converter, ALU [(arithmetic logic unit)], memory, and CPU in the lower layers to realize and intelligent image processor in a multilayered 3-D structure." *Id.*

4. *Petitioner's Showing, Claims 1–22, 36, and 38*

Claim 1's preamble recites "[a] processor module comprising." Petitioner relies on the combined teachings of Zavracky, Chiricescu, and Akasaka as discussed below, and provides evidence that Zavracky discloses a processor module, including a programmable array, memory (RAM), and microprocessor as part of a layered 3-D stacked die

structure. *See* Pet. 21 (citing Ex. 1003, 5:19–23, 12:12–38, Figs. 12–13; citing Ex. 1002 ¶¶ 282–

288).

Claim 1 recites limitation [1.1], "at least a first integrated circuit die element including a programmable array." *See* Pet. 22. Petitioner contends that the combined teachings of Zavracky and Chiricescu render the limitation obvious. *Id.* at 22–24. Petitioner relies on Zavracky's "programmable logic array 802" and notes that Zavracky states "[t]he array can be formed in any of the layers of a multilayer structure." *Id.* (quoting Ex. 1003, 12:28–38; 1002 ¶¶ 290–299).[14] Petitioner also quotes Zavracky as stating "[t]he present invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, . . . vertically stacked and interconnected circuit elements for . . . programmable computing." *Id.* at 24–25 (quoting Ex. 1003, 2:2–6). Zavracky states that "[e]ach circuit layer can be fabricated in a separate wafer . . . and then transferred onto the layered structure and interconnected." Ex. 1003, code (57).

Even if Zavracky does not disclose "a programmable array . . . programmable as a processing element," Petitioner contends that "Chiricescu explicitly cites and characterizes Zavracky as teaching a way that 'allows us to design individual CMOS circuits and stack them to build 3-D

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[14] Referring to its analysis of claim 2, Petitioner contends that "the POSITA would have understood Zavracky to be describing a **programmable** array called a field **programmable** gate **array** (F**P**G**A**), which provides the programmable array element." *See* Pet. 23 & n.3 (citing Ex. 1002 ¶¶ 290– 99).

layered FPGAs.'" Pet. 23–24 (emphasis omitted) (citing Ex. 1004, II- 232). According to Petitioner, "Chiricescu then describes a 3-D chip comprising FPGA, memory, and routing layers. A FPGA, or field programmable gate array, provides "a programmable array." *Id.* at 24.

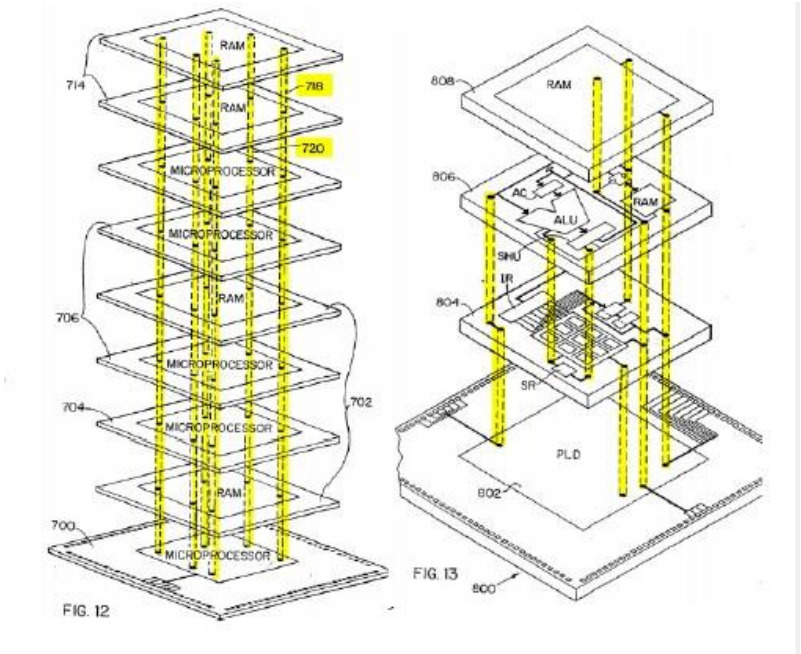
Noting that Zavracky's teaches that the array (FPGA) can be in any layer (*see* Pet. 23 (citing Ex. 1003, 12:28–38)), Petitioner also quotes Zavracky as teaching that "[i]nter-layer connections . . . can be placed anywhere on the die and therefore are not limited to placement on the outer periphery . . . . Inter-layer connection is achieved with a minimal loss of die space." *Id.* at 22 (quoting Ex. 1003, 6:43–65). Petitioner contends that "Chiricescu's teachings, suggestions, and motivations of reconfiguring a FPGA with a stacked memory to accelerate processing and reconfiguration of the FPGA would have prompted a POSITA to pursue a combination with Zavracky." *Id.* at 17 (citing Ex. 1002 ¶¶ 212–232). Petitioner explains that "[i]ntegrating the FPGA structure and reconfiguration scheme from Chiricescu would have produced the result forecast by Zavracky, wherein the programmable logic device "can be programmed to provide for userdefined communication protocol[s]." *Id.* at 20 (citing Ex. 1003, 12:29– 39; Ex. 1002 ¶ 231).

Petitioner also contends that "Chiricescu . . . explicitly references and uses the interconnections of Zavracky." *Id.* (citing Pet. § VII.A.2); *see supra* § II.D.2 (noting that Chiricescu cites and discuses Zavracky). Petitioner also contends that "[a] POSITA's background knowledge in 2001 included knowing to stack various types of die elements together to form 3-D stacked ICs using vertical

interconnects," and would have known that stacking chips with such interconnects would "minimize latency between the device and chips and . . . maximize bandwidth." *Id.* at 7–8 (citing Ex. 1025, 7:18–25, Fig. 22; Ex. 1002 ¶¶ 41–43).

Claim 1 recites elements [1.2] "at least a second integrated circuit functional die element with and electrically coupled to said programmable array of said first integrated circuit die element" and [1.3]: "wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements."

Petitioner's annotated version of Zavracky's Figure 13 depicts stacked functional elements and the coupled contact points relied upon by Petitioner (*see* Pet. 22):



Zavracky's Figures 12 and 13 above as annotated by Petitioner portray (highlighted) inter-layer via connections and one or more second integrated circuit (IC) functional elements, respectively microprocessors 704, 706 and memory 702, and memory 808 (RAM) die, and microprocessor dies 804 and 806, stacked above programmable logic array 802 (FPGA). *See* Pet. 22–25.

As noted above, Petitioner provides evidence that "Zavracky teaches that 'openings or via holes' inter-layer connections 'can be placed anywhere on the die and therefore are not limited to placement on the outer periphery.'" *See* Pet. 26–27 (citing Ex. 1003, 6:43–47, 13:43–46, 14:56– 63). For example, Petitioner quotes Zavracky as teaching "integrated circuits, and in particular, to vertically stacked and interconnected circuit elements," "a multitude of individual dies"; and "connections placed anywhere on the die." *See id.* at 24 (citing Ex. 1003, 2:2–6, 4:63–67, 6:46–47).

Petitioner also relies on and quotes similar teachings in Akasaka:

> Akasaka, in terms similar to the '035 patent, describes electrical coupling by contact points distributed throughout the surfaces of die elements: "It is possible to exchange signals between upper and lower active circuit layers through via holes in 3-D ICs." Ex. 1005, 1705. "Each active layer is connected electrically through via holes." *Id.*, 1707.

Pet. 26.

Petitioner quotes Akasaka further: "Several ***thousands or several tens of thousands of via***

holes are present in these devices, and many information ***signals can be transferred from higher to lower layers*** (or vice versa) through them." Pet. 26 (quoting Ex. 1005, 1705) (emphasis by Petitioner). Petitioner further contends that in Akasaka, "[t]he contact points on the surface of the die are created by 'etching [the] via holes.'" *Id.* (citing Ex. 1005, 1707; citing Ex. 1002 ¶¶ 327–332).

Petitioner provides several reasons to combine the reference teachings to suggest providing numerous via holes between stacked dies or chips according to Zavracky, Chiricescu, and Akasaka. *See* Pet. 16–20. For example, Petitioner describes Akasaka's vertical via connections as resulting in "greatly improved" "processing speed" due "parallel processing" and "shorter interconnection delay time":

> Akasaka teaches that these "tens of thousands of via holes" permit parallel processing by utilizing the many interconnections. [Ex. 1005, 1705.] As a result of this parallel processing, "the signal processing speed of the system will be greatly improved." [*Id.*] Due to "shorter interconnection delay time" arising from stacking and "parallel processing" made possible from the area-wide interconnects, Akasaka states that "twice the operating speed is possible in the best case of 3D ICs" as compared to conventional designs. *Id.*

Id. at 16.

Petitioner also points out that Akasaka teaches that "tens of thousands of via holes' permit parallel processing, and that use of the 'via holes in 3-D ICs' shortens the interconnection length between IC die elements so that 'the signal processing speed of the

system will be greatly improved.'" Pet. 16 (quoting Ex. 1004, 1705). In addition, Petitioner argues that "the POSITA knew of the need for replicated 'common data memory' in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence." *Id.* at 19–20 (citing Ex. 1002 ¶ 236; Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25).

Petitioner generally relies on the "Zavracky-Chiricescu-Akasaka Combination" as "provid[ing] . . . the first and second IC die elements." Pet. 25. As noted above, Petitioner points out that "Chiricescu explicitly references and builds on Zavracky." *Id.* at 18 (citing Pet. § VII.A.2.); *see supra* § II.D.2 (noting the explicit citation to and description of Zavracky in Chiricescu)). Petitioner also contends "that applying Akasaka's distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity." *Id.* at 19 (citing Ex. 1002 ¶ 233; Ex. 1005, 1705). Petitioner also contends that "[t]he POSITA would have sought out Akasaka's connectivity to improve Zavracky's stacks in applications requiring parallel processing. Such applications included image processing algorithms run simultaneously over an entire image in memory." *Id.* (citing Ex. 1002 ¶ 235; Ex. 1048; Ex. 1005; Ex. 1021).

Claim 1 also recites limitation [1.4]: "wherein said contact points traverse said die elements through a thickness thereof." Petitioner refers to its showing with respect to limitation [1.3]. Pet. 28. Petitioner similarly relies on Zavracky's stacked chips interconnected by vias as portrayed in Figures 12 and

13, and further relies on Zavracky's etching teachings for forming via holes:

> Zavracky describes connections made by "[v]ia holes [that] are formed through the upper contact areas to gain access to the lower contact areas. [E]tching [is used] to form the via holes[.]"[] Ex. 1003, 14:58–62. The POSITA would have understood this "etching" created a hole through the thickness of the die to permit busses that "run vertically through the stack"; that is, permit thru-silicon electrical contact. Ex. 1002 ¶¶333–34 (citing Ex. 1003, 12:26; Ex. 1020 ("vertical interconnections are formed using vias etched through the entire wafer"). Zavracky further teaches a continuous connection traversing through the dies, as shown in Figures 12, 13 and other figures These teachings by Zavracky would have been understood by a POSITA as providing for holes—which the '035 patent describes as "contact points"—that "traverse said die elements through a thickness thereof." *Id.*

Pet. 28. Petitioner also relies on the combined teachings of Zavracky, Chiricescu, and Akasaka, based on its reasons to combine as summarized above. *See* Pet. 28–29 (citing Ex. 1005, 1704–07; Ex. 1004, II-232, Fig. 1; Ex. 1002 ¶ 334).

Claim 2 depends from claim 1 and recites "wherein said programmable array of said first integrated circuit die element comprises an FPGA." Petitioner generally refers to the "[t]he Zavracky-Chiricescu- Akasaka Combination" as it does for claim 1. *See* Pet. 30. Citing the testimony of Dr. Franzon and other evidence, Petitioner relies on Zavracky's PLD

(programmable logic device) 802 at the bottom of the stack in Figure 13 as an FPGA. *Id.* at 29–31 (citing Ex. 1002 ¶¶ 292–297; Ex. 1035, 1:29–30; Ex. 1036, 4:1–9; Ex. 1037, 1:13–22; Ex. 1038, code (57) (describing "transistors of a programmable logic device (PLD), such as a field programmable gate array (FPGA)").

Petitioner relies on other teachings, including Chiricescu's teachings, including its "sea-of-gates" FPGA layer, and the knowledge of an artisan of ordinary skill, to show that Zavracky's PLD is or at least suggests an FPGA based on Chiricescu's FGPA teachings. *See* Pet. 30 (citing 1002 ¶¶ 294– 297; Ex. 1004, II-232; Ex. 1040; Ex. 1051). Petitioner also generally relies on reasons for combining the references as outlined above with respect to claim 1 to suggest modifying Zavracky's 3-D stack (memory, processor, FPGA) based on Chiricescu's layer/stack teachings (FPGA, memory). *See id.* at 30–31 (citing Pet. §§ VII.A.2, VII.A.4). Petitioner also notes that Chiricescu specifically describes Zavracky's teachings (*see supra* § II.D.2) as useful for providing 3-D FPGA stacks. *See id.* at 30 ("Chiricescu literally describes Zavracky as teaching technology 'to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip'" (quoting Ex. 1004, II-232)).

Claim 3 depends from claim 1 and recites "[t]he processor module of claim 1 wherein said second integrated circuit die element comprises a microprocessor." Petitioner relies on its showing with respect to claim 1, which relies on Zavracky's examples of microprocessors with "each microprocessor on its own die element (Figure 12) or

using a multi-layer microprocessor (Figure 13)." Pet. 31.

Claim 4 depends from claim 1 and recites "[t]he processor module of claim 1 wherein said second integrated circuit die element comprises a memory." Petitioner refers to its showing for claim 1 and contends that "Zavracky's Figure[] 12 and Figure 13 describe[] layers (comprising integrated circuit die elements per analysis in [1.1]) that comprise a memory, including by describing: 'random access **memory** on the fourth layer 808' also referred to as a 'memory array.'" Pet. 32 (citing Ex. 1003, Fig. 10, 11:63–65 ("memory may be stacked on top of the multi-layer microprocessor."), Fig. 12, 12:15–28 ("random access memory array"), Fig. 13, 12:33–35).

Claim 5 depends from claim 1 and recites "[t]he processor module of claim 1 further comprising: at least a third integrated circuit die element stacked with and electrically coupled to at least one of said first or second integrated circuit die elements." Petitioner refers to its showing for claims 1, 3, and 4, and explains that "the Zavracky-Chiricescu-Akasaka Combination provides that the microprocessor, memory, and programmable array die elements, are 'stacked with and electrically coupled to' each other, providing the additional limitation[s]." In particular, Zavracky describes stacks with at least three layers wherein the die elements are stacked and electrically coupled." Pet. 33 (citing Ex. 1002 ¶¶ 313–326; Ex. 1003, Fig. 13). In other words, Petitioner's showing for claim 5 summarizes the added limitations recited in claims 3, 4, and 6 by reference primarily to the memory, FPGA, and processor stack as depicted in Zavracky's Figure 13. *See id.* at 31–33.

Claim 6 depends from claim 5 and recites Petitioner "[t]he processor module of claim 5 wherein said third integrated circuit die element comprises a memory." Petitioner refers to its showing with respect to claims 4 and 5, as summarized above. Pet. 33 (citing Ex. 1003, Fig. 13.; Ex. 1002

¶¶ 318, 322) .

Claim 7 depends from claim 1 and recites "[t]he processor module of claim 1 wherein said programmable array is reconfigurable as a processing element." Petitioner relies on Zavracky's statement that the "**programmable** logic array 802 . . . can be **programmed** to provide for **user-defined** communication protocol." Pet. 33 (citing Ex. 1003, 12:28– 38). Petitioner explains that

> [a] POSITA would have understood that Zavracky's programmable array—when programmed (or reconfigured) according to the user-defined communication protocol— functions as a processing element. In this configuration, as the POSITA would have understood, the programmable array processes data received from the microprocessor or "off-chip resources" into and out of the user-defined protocol.

Pet. 33–34 (citing Ex. 1002 ¶ 302; Ex. 1040, 319).

Petitioner also relies on one of Chiricescu's touted "key features," namely "that its FPGA can be 'quickly reconfigured' to implement 'arbitrary logic.'" *Id.* at 34 (quoting Ex. 1004, II-234 § 3). Petitioner also relies on Chiricescu's teaching for "reconfiguring the FPGA" wherein the "FPGA is reconfigured from performing AxB to AxC or vice versa." *Id.* (citing Ex. 1002 ¶ 303; Ex. 1004, 234 (the "example shown is the

multiplication of a 4- bit variable")). Citing § VII.A.4 (motivation for combining references) of the Petition, Petitioner contends that "for multiple reasons the POSITA would have been motivated to modify Zavracky's programmable array to do more than process communication data, including to perform math calculations (e.g., multiplication operations in signal processing or image processing, such as taught in Akasaka." *Id.* (citing Ex. 1005, 1704–05, 1707, 1709; Ex. 1002 ¶¶ 229, 235; Ex. 1048; Ex. 1021).

Claim 8 recites "[t]he processor module of claim 1 wherein said die elements are thinned to a point at which said contact points traverse said thickness of said die elements." Petitioner relies on "[t]he Zavracky- Chiricescu-Akasaka Combination" as its basis, supplemented by the general knowledge of the artisan of ordinary skill, as evidenced by an admission in the '035 patent. *See* Pet. 34–37.

The relied-upon admission from the '035 patent follows:

> Tru-Si Technologies of Sunnyvale, Calif. (http://www.trusi.com) has developed a process wherein semiconductor wafers may be thinned to a point where metal contacts can traverse the thickness of the wafer . . . [.] By using a technique of this type in the manufacture of microprocessor, cache memory and FPGA wafers, all three die, or combinations of two or more of them…

Id. at 35 (quoting Ex. 1001, 2:19–30).

Petitioner also points to evidence in the "the '035 original patent's file wrapper" as disclosing this known wafer thinning technique. *Id.* (citing Ex. 1012, 88 (teaching "thru-silicon . . . vias [wherein] the wafer

is thinned . . . carefully exposing the deep thru-silicon vias."), 108 ("[T]he wafer is simply thinned until the contacts are exposed.")). In other words, Petitioner relies on the knowledge of the ordinarily skilled artisan as evidenced by the admission in the '035 patent and Exhibit 1012 such an artisan would have been aware of the technique of thinning die elements as recited in claim 8. Petitioner lists several reasons to employ this general knowledge to Zavracky's modified 3-D stack, including to allow "many die element layers to fit within a standard size package." *See id.* at 36–37.[15] Petitioner provides evidence of predictability and a reasonable expectation of success based on this general knowledge supplemented by the testimony of Dr. Zavracky. *See id.* (citing Ex. 1002 ¶¶ 262–66; Ex. 1012, 107 ("It is now mandatory to thin . . . to fit chip stacks inside standard-size 3-D packages"), 104 ("The goal of the technology . . . is to create a stack of 10 wafers equal to the height of a single wafer."); Ex. 1020)). Petitioner also explains that Zavracky "suggest[s] . . . a need for thin stacks and contact point traversal," which "would have motivated the POSITA to employ the general knowledge of thinning to expose thru-silicon vias." *Id.* at 36 (citing Ex. 1002 ¶ 265; Ex. 1003, 13:55–60).[16]

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[15] The admitted prior art here evidences the knowledge of the ordinary artisan and does not form the "basis" of the rejection. *Cf. Apple Inc. v. Qualcomm Inc.*, 2022 WL 288013, slip op. at *5 (Fed. Cir. Feb. 1, 2022) (holding that that applicant admitted prior art (AAPA) may not form the "basis of a ground in an *inter partes* review because it is not contained in a document that is a prior art patent or prior art printed publication.").

[16] On its face, claim 8 recites a product-by-process limitation and reads on the combination of Zavracky, Chiricescu, and Akasaka as evidenced by Petitioner's showing with respect to claim 1.

Independent claim 9 is a system claim. As Petitioner contends, "[c]laim 9 takes limitations from claim 1 and combines them with a generic processor and memory." Pet. 37. Specifically, claim 9 recites "[a] reconfigurable computer system comprising: a processor; a memory;" and "at least one processor module" that materially recites the same limitations as the "processor module" of claim 1. The processor module of claim 1 reads on the "Zavracky-Chiricescu-Akasaka Combination" as determined above. Other than at most implying some type of electrical connection through the recitation of "a reconfigurable computer system comprising" in the preamble, claim 9 does not specify any electrical communication between the processor, memory, and "processor module."

Petitioner contends that "Zavracky-Chiricescu-Akasaka Combination in further combination with general knowledge of the POSITA renders obvious claim [9]." Pet. 37. Petitioner explains that the "the Zavracky- Chiricescu-Akasaka Combination teaches the use of numerous microprocessors and numerous memories – any of which can satisfy the additional requirement for one more processor and one more memory in claim 9, and indeed, the teachings of Figure 13 already shows such a reconfigurable computer system." *Id.* "Beyond this," Patent Owner contends that a person of ordinary skill would have

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That is, "said contact points [of the Zavracky-Chiricescu-Akasaka stack] traverse said thickness of said die elements." *See* Ex. 1005, Fig. 4 (vias traversing die elements); Ex. 1003, Fig. 13 (same). Therefore, by definition, "said die elements [of claim 1] are thinned to a point at which said contact points traverse said thickness of said die elements."

known to connect an FPGA of the Zavracky-Chiricescu-Akasaka Combination in a system with memory and a processor as evidenced by admissions in the '035 patent, including admitted prior art Figure 1, which shows a "prior art 'MAP^{TM,} element . . . taught to 'comprise a field programmable gate array "FPGA" [and] read only memory.'" *Id.* at 37–38 (quoting Ex. 1001, 3:22–24; citing *id.* at Fig. 1). Petitioner points out that admitted prior art Figure 1 is one example that evidences the general knowledge of an artisan of ordinary skill, and "[t]he general knowledge of the POSITA would have other examples of reconfigurable computer systems with a processor, memory, and processor module." *Id.* at 38 (citing Ex. 1002 ¶¶ 267–73, 289; 1026).[17]

Petitioner contends that prior art Figure 1 shows microprocessor 12 and system memory 16 coupled electrically with the MAP^{TM} (which includes an FPGA). Pet. 38 (annotating Ex. 1001, Fig. 1). Petitioner asserts that it would have been obvious to employ the Zavracky-Chiricescu-Akasaka 3-D stack in a system with processor and memory in order to configure the FPGA using off-chip resources during start-up with a reasonable expectation of success where such systems were well-known. *See id.* at 38–39 (citing Ex. 1003, 12:37; Ex. 1002 ¶¶ 272–73; Ex. 1004, II-234 (describing "during the initiation phase

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[17] In other words, the admitted prior art here evidences the knowledge of the ordinary artisan and does not form the "basis" of the rejection. *Cf. Apple Inc.*, 2022 WL 288013, slip op. at *5 (holding that that applicant admitted prior art (AAPA) may not form the "basis of a ground in an *inter partes* review because it is not contained in a document that is a prior art patent or prior art printed publication.").

of the application . . . loading configuration data . . . from memory off-chip")).

Independent claim 17 is materially similar to claim 1 but includes at least a third integrated circuit die element in addition to the at least first and second integrated circuit die elements, with the three die elements electrically coupled by contact points distributed throughout the surfaces of the die elements and extending through a thickness thereof. To address claim 17, Petitioner primarily relies on its analysis of claims 1, supplemented by its analysis of claims 3, 5, and 6, which we address below. *See* Pet. 41–43.

Independent claim 36 is similar to claim 17 but broader in that the at least third integrated circuit die element electrically couples only to at least one of the other two die elements. To address claim 36, Petitioner relies on its analysis of claims 1 and 23. Pet. 53.

Dependent claims 10–16 and 18–22 recite limitations that track the limitations addressed above in claims 1–6, 8, and 9. Petitioner refers to its showing with respect to claims 2–6, 8 and 9 to address these claims. *See* Pet. 36–40, 43–44. As such, the Petition relies on the combined teachings of Zavracky, Chiricescu, and Akasaka, as teaching or suggesting these added well-known circuit or die elements and their functionality by relying on specific teachings in the references, supported by the knowledge of an artisan of ordinary skill (evidenced partly by admissions in the '035 patent) and the testimony of Dr. Franzon, and setting forth rationale and reasons to combine, where appropriate. *See id.* at 36–40, 43–44.

Dependent claim 38 recites "[t]he programmable array module of claim 36 wherein said third integrated circuit die element includes an I/O controller." Petitioner relies on Zavracky's "'controller' as controlling connections 'to and from the common data bus' and containing 'arbitration logic, hosted in the controller [run] in accordance with [a] bus arbitration protocol.'" Pet. 54 (quoting Ex. 1003, 5:54–60). According further to Petitioner, Zavracky's Figures 1 and 13 illustrate the same or similar controller, and Zavracky discloses a bus controller that arbitrates logic under a bus arbitration protocol to communicate with off-chip resources as "a third IC die element." *See id.* at 54–55 (citing Ex. 1002 ¶¶ 324–325; Ex. 1003, 6:58–60). Petitioner alternatively relies on another controller in Zavracky that provides communication protocols between microprocessor and peripheral devices, and contends that "Zavracky teaches that such a programmable I/O controller 'can be formed in any of the layers of a multilayer structure as described elsewhere herein.'" *Id.* at 55 (quoting Ex. 1003, 12:28–38; citing Ex. 1002 ¶¶ 325–326).

We adopt and incorporate Petitioner's showing as to claims 1–22, 36, and 38, as set forth in the Petition and summarized above, as our own. *See* Pet. 7–44, 53–55.

5. *Arguments with Respect to Alleged Obviousness Based on Zavracky, Chiricescu, and Akasaka*

Patent Owner does not argue any of claims 1–22, 36, and 38 individually, but groups various claims together in separate arguments, as discussed below. Sections below address claims 23–35 and 37, although Patent Owner groups some of these claims together

with claims 1–22, 36, and 38 in generic arguments or more specific arguments, so we address some of the more generic arguments in this section and other more specific arguments below. *See infra* §§ II.D.6–8; II.E–G.

Patent Owner argues generally that Petitioner misrepresents the teachings, relies on hindsight to combine the references, and "fails to explain how a POSITA would have combined the references and had a reasonable expectation of success in doing so." PO Resp. 27 (citing Ex. 2011 ¶ 67). Patent Owner also argues that "Petitioner asserts that 'Chiricescu employs Zavracky's principles to solve a known problem with FPGAs—"high configuration time,'" that is simply not true." *Id.* at 28 (quoting Pet. 17). Rather, Patent Owner explains that "*Chiricescu* teaches the use of '***on-chip***' memory to mitigate the time it takes to transfer configuration data from 'off-chip,' rather than making any use of Zavracky's die-area vertical interconnections to transfer configuration data from the 'on-chip' memory into the FPGA." PO Resp. 28 (citing Ex. 1004, 1, 3).

Patent Owner's arguments are unavailing. Both Chiricescu and Zavracky teach memory layers in a 3-D stack to transfer data to FPGAs, as Petitioner persuasively shows as summarized above. *See, e.g.*, Ex. 1003, Fig. 13 (depicting FPGA/PLD 802 in communication by bus with RAM 808); Ex. 1004, Fig. 21 (depicting memory layer in communication with FPGA RLB layer, connected by "vias" "placed anywhere on the chip" according to Zavracky's teachings (i.e., the "Northeastern University") technology)); *supra* § II.D.1–2). Patent Owner attempts to divorce the numerous advantages of using

multiple vias in Zavracky's modified 3–D stack as Petitioner outlines as summarized above, from what Patent Owner implies is separate from the same advantages gained from an "on-chip" memory. There is no support for this line of argument. *See infra* note 20 (discussing the same issue).

In other words, Patent Owner's arguments do not address Petitioner's persuasive reliance on multiple vertical vias in the stacked memory chip structure of Zavracky, as modified by the teachings of Chiricescu and Akasaka, in order to, for example, "improve Zavracky's stacks in applications requiring parallel processing," and "increase bandwidth and processing speed through better parallelism and increased connectivity." Pet. 19 (citing Ex. 1002 ¶ 233; Ex. 1003, 6:43–47; Ex. 1005, 1705; Ex. 1021; Ex. 1048); *see also id.* at 7–12, 16–28 (similar showing). For example, Petitioner persuasively notes that "[t]he POSITA would have known [about] many references teaching stacked dies with thousands of distributed connections. *Id.* at 20 (citing Ex. 1002 ¶¶ 238–239; Ex. 1020; Ex. 1021). Discussing Akasaka, Petitioner persuasively contends that Akasaka teaches that "tens of thousands of via holes" permit parallel processing by utilizing the many interconnections. *Id.* at 16 (citing Ex. 1005, 1705). Petitioner adds that

> [a]s a result of this parallel processing, "the signal processing speed of the system will be greatly improved." Due to "shorter interconnection delay time" arising from stacking and "parallel processing" made possible from the area-wide interconnects, Akasaka states that "twice the operating speed is possible in the best

> case of 3D ICs" as compared to conventional designs.

Id. (quoting Ex. 1005, 1705; citing Ex. 1005, Fig. 4).

With respect to all challenged claims, Patent Owner also argues that "Petitioner and Dr. Franzon fail to explain how a POSITA would have integrated Akasaka's thousands of distributed contact points with Zavracky- Chiricescu's design to achieve the claimed 3-D processor modules and would have had a reasonable expectation of success in doing so." PO Resp. 38 (citing Ex. 2011 ¶ 79). According to Patent Owner, "Petitioner and Dr. Franzon concede that *Zavracky* and *Chiricescu* both disclose only a small number of interconnect paths (e.g., the address and data buses) that provide for vertical communications between functional blocks (such as memory elements, logic unit, etc.) of the multi-layer microprocessor." *Id.* (citing Ex. 1003, 11:62–12:39; Ex. 1004, 1–2). According further to Patent Owner, "Dr. Franzon's analysis, like Petitioner's analysis, seems to say no more than that a POSITA would have understood that the references ***could be*** combined." *Id.* at 40 (citing Ex. 1002 ¶ 239). Patent Owner also asserts that "[a]t the time of the invention, a POSITA was aware of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ('HDL') algorithms, which must be considered." *Id.* at 41 (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89).

Patent Owner's arguments are unavailing. As discussed above, Petitioner persuasively relies on the knowledge of the artisan of ordinary skill and the combined teachings of Zavracky, Chiricescu, and Alexander supported by specific reasons and rational

underpinning to show how and why the combination teaches or suggests increasing the number of contact points or via holes for electrically coupling FPGA, memory, and processors together to allow for parallel data transfers with a reasonable expectation of success.

As indicated above, Zavracky already specifically describes connecting several bus lines (depicting 4 in Fig. 13) from the FPGA/PLD to other circuits, including memory and a processor. *See* Pet. 13. Zavracky indicates that 32 bit microprocessors were routine in 1993, years before the effective date of the invention, indicating that Zavracky's microprocessor buses at least handled 32 bits in parallel. Viewed through the lens of an artisan of ordinary skill at the time of the invention of the '035 patent, Zavracky's disclosure indicates the ability to handle known microprocessors, memories, and FPGAs, whatever the capabilities of those devices and bus widths were. *See* Ex. 1003, 1:6–8 (continuity date of 1993), 31–40 (discussing prior art microprocessors). Moreover, Petitioner shows a number of other stacked dies or layers with multiple connections, including Akasaka (Ex. 1005, Fig. 4), Franzon (Ex. 1020, Fig. 4), Koyanagi (Ex. 1021, Fig. 1(a)), and Alexander (Ex. 1028, Fig. 2(g). *See* Pet. 26–27. As discussed further below, Trimberger (Ex. 1006) shows parallel loading by "*flash reconfiguring* all [100,000] bits in logic and interconnect array [i.e., an FPGA] . . . simultaneously from one memory plane," further evidencing a

reasonable expectation of success. *See infra* § II.E.1 (quoting Ex. 1006, 22).[18]

And also as noted above, Patent Owner concedes Zavracky and Chiricescu each show how to connect "memory, logic, etc." using "address and data buses," albeit on what Patent Owner describes as "only a small number of interconnect paths." PO Resp. 38 ("*Zavracky* and *Chiricescu* both disclose only a small number of interconnect paths (e.g., the address and data buses) that provide for vertical communications between functional blocks (such as memory elements, logic unit, etc.) of the multi-layer microprocessor.") But Patent Owner also agrees that the number of interconnects is not critical to the claimed invention. *See supra* § II.C (discussing Oral Hearing arguments); Tr. 49:1–9 (answering "yes, . . . if you have a very, . . . small FPGA, the number of bits can be . . . relatively smaller, but what's critical is not the number of bits and . . . . [i]t's not necessarily the number of bits that's in the configuration data port, but how they're arranged").

Notwithstanding Patent Owner's allegation of a lack of a reasonable expectation of success, Patent Owner acknowledges that "[a]t the time of the invention, *a POSITA was aware* of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ('HDL') algorithms." PO Resp. 41 (emphasis added) (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89). Here, the challenged claims are broad and do not

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[18] Petitioner employs Trimberger to address challenged claims 31, 32, and 34 as discussed further below, but it is further evidence of a reasonable expectation of success as it relates to connecting several thousands of bit lines in parallel.

specify a minimal number of interconnections, FPGA size, or chip size that would even raise TSV congestion or other issues. The '035 patent says nothing about interconnection issues or congestion issues. Even if such issues were a consideration and relevant to a reasonable expectation of success given the breadth of the challenged claims, as Petitioner persuasively argues, "[t]he supposed 'TSV interconnection issues' that [Patent Owner] cursorily identifies were at most normal engineering issues, not problems preventing a combination." Reply 20 (citing Ex. 1070 ¶¶ 13– 28 (Dr. Franzon addressing Dr. Souri's testimony as to the purported TSV issues)).

> For example, as Dr. Franzon credibly testifies,
>
> > even if routing congestion or TSV placement were an issue, Kim gives several solutions that would have been known to POSITA, such as to change the TSV "coarseness" or to "increase the chip area to address the placement and routing congestion caused by TSV insertion." [Ex. 2014 (Kim), 85]. But again, the ['035] patent[] and claims are silent on any of these issues; Kim is at worst irrelevant, and at best would have actually encouraged the combination.

Ex. 1070 ¶ 26. With respect to alleged HDL (hardware description language) issues, Dr. Franzon also credibly testifies that

> > Alexander (Ex. 1009) has a whole section titled "Placement and Routing in 3D" (Ex. 1009, p. 256). Alexander names then- existing CAD tools that performed these functions, includingDAGmap and Mondrian. Designing distributed 3D interconnects was a routine engineering problem

> by the time of the Huppenthal Patents, and not an impediment to reasonable expectation of success in making the Zavracky, Chiricescu, Akasaka combination.

Ex. 1070 ¶ 27.

Petitioner provides other evidence that at the time of the invention, an artisan of ordinary skill would have had a reasonable expectation of success in combining the references to arrive at numerous vias connecting circuits (including memory arrays) on stacked chips or circuit layers and to allow for parallel processing or data transfers. *See, e.g.*, Pet. 12 (discussing known wafer processing technology by artisans of ordinary skill (citing Ex. 1002 ¶¶ 262–266; Ex. 1001, 2:29–35; 5:13–18)), 24–25 (pointing to Zavracky's memory as an example vertical integrated circuit on stacked dies connected via connections including vertical buses placed anywhere on the die and providing evidence that "each of the programmable array, microprocessor, and memory are pairwise stacked with and electrically coupled with each other" (citing Ex. 1003, 2:7–8, 2:18–22, 2:27–35, 6:43–63, 10:8–21, 11:63–12:2, 12:13–39, 14:51–63, Fig. 13; Ex. 1002 ¶¶ 278–280)), 25–26 (further relying on Akasaka as teaching thousands of via holes to connect upper and lower circuit layers (citing Ex. 1005, 1705, 1707; Ex. 1002 ¶¶ 327–332)). Furthermore, the '035 patent describes "recently available wafer processing techniques" including those developed by "Tru-Si Technologies," indicating, for purposes of institution, that artisans of ordinary skill would have been aware of any such wafer processing techniques for forming vias at the time of the invention. Ex. 1001, 2:20–30. Therefore,

Petitioner persuasively shows ample evidence of a reasonable expectation of success.

In addition, as noted above, Patent Owner argued during the Oral Hearing that the number of vias is not important, depending on the size of the FPGA, provided that the contacts allow for parallel processing. *See supra* § II.C (discussing Tr. 49:1–9 (Patent Owner arguing that the number of vias "could be as small as 32 bits . . . if you have a small FPGA, ... [and] [i]f you want to update something in parallel, you could update 32-bit with 32 bits," further stating that "if you have a very . . . small FPGA, the number of bits can be . . . relatively smaller, but what's critical is not the number of bits").

As summarized above, Petitioner provides persuasive motivation with a reasonable expectation of success to explain why a person of ordinary skill would have increased the number of vias using known techniques, relying on teachings that providing multiple vias in stacked chips using conventional via and metallization processing allowed for better processing speeds and reconfiguration times, shorter latency, higher bandwidth, and parallel processing. *See* Pet. 7–12, 16–20; Ex. 1002 ¶¶ 212–239. Dr. Franzon also reasonably shows that the combined teachings of Zavracky and Chiricescu suggest differing "processing tasks . . . [in] co-stacked microprocessors and memories . . . . as good applications for 3-D stacked chips that required parallel computation." Ex. 1002 ¶ 229.

As Petitioner also persuasively notes, Zavracky does not limit the number of connections, contrary to Patent Owner's arguments. For example, Petitioner quotes Zavracky as describing "**inter-layer**

connections [that] provide for vertical communication. . . . [and] [s]uch connections can be placed **anywhere on the die** and therefore are not limited to placement on the outer periphery." Reply 5 (citing Ex. 1003, 6:43–47) (emphasis by Petitioner). Petitioner quotes Zavracky as teaching "buses run vertically through the stack by the use of inter-layer connectors" in describing Figures 12 and 13. *Id.* (quoting Ex. 1003, 12:24–26). Petitioner persuasively explains that "Zavracky visually shows a number of vertical contacts that traverse the memory die in the internal periphery of the die and provide contacts on the surface of the memory die, just as the Board's construction requires." *Id.* at 5–6 (annotating Ex. 1003, Figs. 12, 13).

Patent Owner contends that "Zavracky proposes using these vertical connections 'for the same reasons any lines otherwise restricted to a single layer are used.'" PO Resp. 10 (quoting Ex. 1003, 6:48–49). This argument supports Petitioner, because it shows that an artisan of ordinary skill easily would and could have re-routed planar connections for known circuitry using vias in a stack of chips or layers.

Patent Owner argues that "in *Akasaka*, the 3-D chip design that uses vertical interconnections is only mentioned for a flip-chip design and a monolithic design, which means it is fabricated as a single piece of silicon with multiple layers." PO Resp. 16. Patent Owner argues that "Akasaka explains that among the expected improvements are the use of '[s]everal thousands or tens of thousands of via holes' in monolithic chips to take advantage of parallel processing." *Id.* at 17 (quoting Ex. 1005, 1705). According to Patent Owner, Akasaka's "flip-chip

design is limited . . . in that 'the number of connections are restricted by reliability and bump size constraints.'" *Id.* at 16 (quoting Ex. 1005, 1704).

Contrary to these arguments, Akasaka states that with respect to flip chips, "the number of connections will be greatly increased by this technology." Ex. 1005, 1704. Moreover, Akasaka refers to the flip chip structures in a section titled "3-D IC Structure." *Id.* And contrary to Patent Owner's arguments, Akasaka generally indicates that for all "3-D structures" "[s]everal thousands or several tens of thousands of via holes are present in these devices, and many information signal scan be transferred from higher to lower layers or vice versa through them." *Id.* at 1705; *see also* Reply 20 n.6 (showing that 3-D die stacking with numerous chips was well-known (citing Ex. 1002 ¶¶ 328, 332); *id.* at 21 n. 8 (persuasively showing that Patent Owner "describes Akasaka's teachings inaccurately" (citing Ex. 1002 ¶¶ 233–239; Ex. 1070 ¶¶ 59–66); Ex. 1070 ¶¶ 60–61 (disputing Dr. Souri's testimony and stating that Akasaka shows "vertical interconnections between multiple chips and other chip attachment mechanisms," and testifying that "Akasaka does not limit its via fabrication teachings to two layers or a monolithic chip"); Ex. 1002 ¶ 238 (testifying that chip stacking was known and "[t]here were many references teaching stacked dies with thousands of distributed connections, including those discussed in my technology backgrounder above, Section V, and the papers in Section IX"). Akasaka also indicates that even in 1986, about five years before the 2001 date of the invention, artisans of ordinary skill would have mixed flip chip technology and monolithic technology to provide stacked layers. "Mixing of assembly

technology with monolithic chip technology can also provide 4 layers or 6 layers from 2-layer or 3-layer stacked monolithic ICs, respectively." Ex. 1005, 1713.

Even though claim 1 does not recite the "functional to accelerate" clauses (which claims 23, 24, 30, 32, and 33 recite), as motivation for all claims, as summarized above, Petitioner persuasively relies on Zavracky's teaching that "this approach **accelerates** communication between the dies in the chip by way of '**smaller delays** and **higher speed** circuit performance.'" *See* Reply 6 (emphasis by Petitioner) (quoting Ex. 1003, 3:4–14). Petitioner persuasively notes that Chiricescu describes Zavracky's teachings as "allow[ing] us" to build stacked circuit layers on a chip "with vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip." *See id.* (quoting Ex. 1004, 232). Petitioner also persuasively argues that Chiricescu teaches the recited "functional to accelerate" clauses, with "significantly **improved[d FPGA] reconfiguration time**" through its "interconnected layers, including a memory layer configured as a cache for fast access to 'configuration data . . . from memory off-chip.'" *Id.* at 6–7 (quoting Ex. 1004, 232) (emphasis by Petitioner). Other than disclosing an 8-bit configuration port as prior art with respect to Figure 3, the '035 patent does not specify how many via interconnections the claimed "accelerate" functionality requires. *See* Ex. 1001 2:55–61 (describing stacking an FPGA with a "memory die" "for the purpose of accelerating FPGA reconfiguration" and "for the purpose of accelerating external memory references" and stacking "a microprocessor, memory and FPGA . . . for the purpose of accelerating the sharing of data"), 4:31–35

(describing cache memory purpose of serving "its traditional role of fast access memory").

Patent Owner limits Chiricescu as teaching only "the use of 'on-chip' memory to mitigate the time it takes to transfer configuration data from 'off- chip,' rather than making any use of Zavracky's die-area vertical interconnections to transfer configuration data from the 'on-chip' memory into the FPGA." *See* PO Resp. 28 (citing Ex. 1004, 1, 3). Patent Owner also argues that "[n]either *Zavracky* nor *Chiricescu* even contemplate using die- area inter-layer vertical interconnections to move data between a programmable array and a memory, such as is recited in Claims 4, 9, 14, 20, and 23–28." *Id.* (citing Ex. 2011 ¶ 66). The record does not support this line of argument. As discussed above, Zavracky's Figure 13 shows that Zavracky contemplates moving data on vertical buses between RAM memory 808 (and RAM memory on processor layer 806) and programmable array 802 (Ex. 1003, 12:29–39), and Chiricescu's Figure 2 shows that Chiricescu contemplates moving data on "vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip" (based on Chiricescu's characterization of Zavracky) between memory layer and the "sea of gates FPGA" RLB layer (Ex. 1004, II-232); *see also* Ex. 1004, II-232 § 1 ("Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.").

Also, Petitioner shows persuasively an artisan of ordinary skill would have recognized that speed improvement emanates partly from shorter interconnection distances and/or parallel processing using a larger number of vias (as compared to

connections on the same plane). *See* Reply 6 (arguing Zavracky's "approach **accelerates** communication between the dies in the chip by way of '**smaller delays** and **higher speed** circuit performance'" (emphasis by Petitioner (quoting Ex. 1003, 3:4–14)), and arguing that "Zavracky's short interior 'inter-layer connectors' to stacked 'random access memory . . . results in **reduced** memory access **time**, **increasing the speed** of the entire system.'" (emphasis by Petitioner (quoting 11:63–12:2)).

Patent Owner concedes that the "[t]he '951 Patent provides accelerated external memory references due to its technique of stacking a programmable array with a memory die using through-silicon vias (TSVs)," and Patent Owner quotes the '951 patent as providing "increased" "bandwidth" and providing the "traditional role of fast access memory." *See* PO Resp. 19–20 (quoting Ex. 1001, 4:31–44). These arguments support Petitioner's showing, because the combined Zavracky-Chircescu-Akasaka stack includes the same structure, including numerous vias, as the short via connections as disclosed in the '035 patent.

Patent Owner agrees that "*Chiricescu* says . . . [that] '[t]he elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application.'" Sur-reply 5 (quoting Ex. 1004, 234). However, Patent Owner argues that "Petitioner concocts its hypothetical structure based on its demonstrably false claim that *Chiricescu's* improved FPGA reconfiguration time 'is achieved by its interconnected layers, including a memory layer configured as a cache for fast access to "configuration

data . . . from memory off-chip."'" *Id.* at 4 (quoting Reply 6–7; last internal quote quoting Ex. 1004, 234). Patent Owner contends that "*Chiricescu* says just the opposite." *Id.* at 5 (citing Ex. 1004, 234).

Contrary to this line of argument, Patent Owner mischaracterizes Petitioner's showing. Petitioner shows that Chiricescu improves FPGA reconfiguration time because Chiricescu's cache pre-stores and holds configuration data on-chip that it obtains from an external source (i.e., off- chip memory)—so that the FPGA (in Zavracky and Chiricescu) need not access that external (off-chip memory) source to load the FPGA through a "typical narrow configuration data port" (Sur-reply 5) during FPGA reconfiguration. *See* Reply 6–8; Ex. 1004, II-234 ("The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application."); *infra* § II.D.6 (discussing Petitioner's reliance on Chiricescu's cache memory teachings).[19]

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[19] Throughout its briefing, Patent Owner limits all "on-chip" advantages to a *single die* and confuses issues by arguing that even chips in the same stack are "off-chip" relative to each other, such that all "off-chip" vias are part of a "narrow" data port—even with thousands of vias connecting chips in the same stack as proposed by Petitioner. On the other hand, Petitioner, like Zavracky, generally refers to "off-chip resources" to include a resource outside of a *chip stack*. *See e.g.*, Pet. 34 ("[T]he the POSITA would have understood, the programmable array [of Zavracky] processes data received from the microprocessor or 'off-chip resources' into and out of the user- defined protocol."); Ex. 1003, 5:53–54 ("Paths which connect off-chip are routed to bonding pads 226 [Fig. 1], which are bonded to the chip carrier pins."); Ex. 1070 ¶ 44 (Dr. Franzon noting that "Dr. Souri apparently means 'chip' here as limited to a single die."). Patent Owner exploits this difference of use in the terminology to

Addressing claims 4, 9, 14, 20, and 23–38 as a group, Patent Owner argues that "neither Zavracky nor Chiricescu even contemplate using die- area inter-layer vertical interconnections to move data between a programmable array and a memory, such as is recited in Claims 4, 9, 14, 20, and 23–38." PO Resp. 28. As noted in summarizing Petitioner's analysis of claim 4 above, claim 4 recites "[t]he processor module of claim 1 wherein said second integrated circuit die element comprises a memory." *See* Pet. 32. Claim 4 does not specifically require moving data between a programmable array and a memory or even the capability to do so. Claim 9 does not specifically recite

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confound issues, characterizing, for example, Dr. Franzon's testimony as follows: "Dr. Franzon's testi[ies] that '*off-chip* access [*e.g.*, *off-chip* memory *separate from the FPGA die*] can't be, for example, 100,000 bits wide." Sur-reply 9 (emphasis added) (second bracketed information by Patent Owner). As another example, Patent Owner argues that Petitioner "rel[ies] on Dr. Franzon's discussion that thousands of interconnections for *off-chip* access of a 3D stacked structure is not feasible." *Id.* (emphasis added (citing Reply 18)). This conflation represents the opposite of Dr. Franzon's testimony and Petitioner's showing. The thrust of Dr. Franzon's testimony and Petitioner's showing is that numerous stacked via connections in a stack of chips (dies) or layers of a single chip are better (faster) than connections on the same plane. *See, e.g.*, Reply 17–18 (characterizing Dr. Franzon's testimony as "noting the routine use of on-chip area-wide connections in 3D stacks, including his prior work." (citing Ex. 1020; Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68)); Ex. 1070 ¶ 44 ("But a POSITA would have recognized that [a] 3D chip that consists of multiple dies would do a better job than the 2D chip and provid[e] fast large connectivity. . . . The point here is that a shorter vertical interconnect allows for a shorter 'longest path' and a faster chip. This was commonly understood in the other art as well. . . . [such as] Akasaka's . . . 3-D 'high speed performance'" (citing Ex. 1005, 1705)).

a connection between the programmable array (FPGA) and memory—it recites a "system" in the preamble that includes those components. Claims 23, 24, and 28 also do not specifically require moving data between a programmable array and memory. *See* Pet. 44–47, 50 (addressing these claims); *infra* § II.D.6–8 (summarizing and addressing Petitioner's showing and Patent Owner's arguments for claims 23, 24, and 28). Rather, claim 23 and dependent claims 24 and 28 recite "a memory array stacked with and electrically coupled to said field programmable gate array." Instead of a data transfer to or from memory, claim 25 recites "whereby *said processor* and said programmable array are operational to share data therebetween" (emphasis added). *See* Pet. 48–50; *infra* II.D.8. Although claim 25 recites a "reconfigurable processor" in the preamble, this is broad enough to include the capability for reconfiguration from an external memory source (i.e., external to Zavracky's stack). Dependent claim 26 recites "[t]he reconfigurable processor module of claim 25 wherein said memory is operational to at least temporarily store said data," so it may imply some ability to move shared data to memory as discussed above. *See infra* § II.D.8. Claims 36 and 38 recite electrical coupling between an FPGA and memory array, which also implicitly requires the ability to "move data between a programmable array and a memory."

In any event, even assuming a requirement to move data as argued, Patent Owner's arguments are unavailing. As summarized above in connection with claim 1, Petitioner shows that Zavracky's Figure 13 specifically shows via bus connections (i.e., electrical coupling) from PLD 802 to microprocessor 804/806,

RAM memory 808, and also RAM memory associated with microprocessor 806. Ex. 1003, Fig. 13, 12:29–39; *supra* § II.4.

Chiricescu also shows electrical coupling between a memory layer and FPGA layer for configuring the FPGA, as Petitioner also shows. *See, e.g.*, Pet. 15–16 (showing that "Chiricescu . . . describes configuring the FPGA as a processing element ('multiplication of a 4-bit variable,' . . . and accelerating the reconfiguration of the FPGA as a processing element by utilizing the on-3D-chip memory to 'significantly improve[] the reconfiguration time'" (quoting Ex. 1004, II-234)). Moreover, Petitioner relies on the combined teachings of the references and shows persuasively that moving data using numerous inter-layer vias was well-known to produce distinct increased speed advantages, as noted above and below in connection with claims 1 and 23–29. *See supra* II.D.4; *infra* §§ II.D.6–8. Also, with respect to independent claim 9, as summarized above (§ II.D.4), Petitioner shows that it would have been obvious and well-known by artisans of ordinary skill for systems to move or transfer data between an FPGA and memory. *See* Pet. 38 (showing data bus lines between the recited claim elements in admitted prior art Figure 1 of the '035 patent as evidencing the knowledge of the skilled artisan and relying on Zavracky's teachings for its similar showing).

Patent Owner addresses claims 3, 11, 19, and 28 as a group. These dependent claims recite "wherein said second integrated circuit die element comprises a microprocessor" or "wherein said processor of said second integrated circuit die element comprises a microprocessor." Patent Owner argues that because

Chiricescu discloses storing configuration data in on-chip memory, removing data "from the microprocessor cache and plac[ing it] in the FPGA's on-chip memory," per "the approach of *Zavracky- Chircescu*," "mak[es] it ***much harder*** for the microprocessor, as recited in Claims 3, 11, 19, and 28." PO Resp. 28–29 (citing Ex. 2011 ¶ 67). Patent Owner contends that this approach "result[s] in significantly **decreased** processing speeds for any data that might be shared between *Chiricescu's* FPGA and *Zavracky's* microprocessor, thus not leading to an improvement in the reconfiguration time." *Id.* at 29.

These arguments do not address Petitioner's showing and the scope of claims 3, 11, 19, and 28. None of the claims require, and Petitioner does not propose, removing data from a microprocessor cache, or removing it and placing it in another on-chip memory. *See* Pet. 31–32, 40, 43, 50. Here, Patent Owner explains that Chiricescu's FPGA and Zavracky's microprocessor and FPGA "might" share data by using Zavracky's microprocessor cache memory. *See infra* § II.D.8.[20] Assuming this is correct, Petitioner relies generally on a Akasaka's teachings as motivation to provide a separate memory layer to provide cache coherence. Pet. 19–20 (arguing that "the POSITA knew of the need for replicated 'common data memory' in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence" (citing Ex. 1002 ¶ 236; Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25). Patent Owner's arguments

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[20] This argument contradicts Patent Owner's arguments advanced with respect to claims 25–29 that sharing data between a microprocessor and FPGA from an "on-chip" memory would not have been obvious. *See infra* § II.D.8.

do not address this persuasive rationale, but support it. Petitioner also relies on Chiricescu's cache memory teachings to suggest a separate memory layer in addressing claims 23, 24, 30, 32, and 33. *Infra* § II.D.6, E.2

With respect to Patent Owner's argument that Petitioner does not relate "arbitrary logic functions" to the claimed invention (*see* PO Resp. 29), Petitioner persuasively points out that Dr. Franzon testifies that a "POSITA would appreciate that Chiricescu teaches and praises as one of its 'key features' that its FPGA can be 'quickly reconfigured' to implement 'arbitrary logic.'" *See* Reply 17 (quoting Ex. 1002 ¶¶ 215–217). In other words, in context, Petitioner persuasively shows that changing logic functions by reconfiguring (i.e., on the fly) an FPGA in stacked dies or layers using numerous distributed via connections to memory increases reconfiguration speed and produces other benefits, including the ability to perform different logic functions quickly. *See* Pet. 17–18. As another example, Petitioner argues persuasively that "[i]mproved reconfiguration times through this integration would predictably mitigate undesirable packet flow interruption when reconfiguring." *Id.* Petitioner also persuasively argues that "a POSITA would have taken Chiricescu's suggestion of a[n] FPGA to perform 'arbitrary logic functions,' Ex. 1004, 233, as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in Zavracky, e.g., to perform image and signal processing tasks that would have taken advantage of co-stacked microprocessors and memories as taught in Zavracky." *Id.* at 19 (citing Ex. 1002 ¶¶ 229–30; Ex. 1005, 1705; Ex. 1003, 12:25–30; Ex. 1004, II-232;

Ex. 1058, 41; Ex. 1048)).

Addressing claims 1–38 as a group, Patent Owner argues that Petitioner fails to show the obviousness of connecting "large numbers of vertical interconnections between an IC die with a programmable array and any other type of die." PO Resp. 41. Contrary to this argument, which repackages arguments addressed above, Petitioner shows it would have been obvious for the reasons noted and well within the skill of an ordinary artisan. *See* Reply 16–19; Pet.19–20 (citing, *inter alia*, Ex. 1002 ¶¶ 237–38, 41–51 (citing and describing additional successful prior art including art with programmable arrays)); *supra* § II.D.4; *infra* § II.D.6, 8.

Patent Owner contends that "merely disclosing the availability of large numbers of vertical interconnections between IC dies (as Akasaka does), does not demonstrate that a POSITA would or could have employed those interconnections between a programmable array and any other type of IC die with a reasonable expectation of success." PO Resp. 41–42. To support this argument, Patent Owner argues that "the '035 Patent itself does not purport to have invented TSVs (or any other types of 'contact points distributed throughout the surfaces of said die elements . . . [which] traverse said die elements through a thickness thereof')." *Id.* at 42 (citing Ex. 1001, 2:19–23). Advancing this point, Patent Owner admits that the '035 patent "disclos[es] that the various embodiments of the '035 Patent were enabled by Tru-Sci Technologies' process." Patent Owner similarly argues that it invented "use cases for such

contact points (e.g., interconnecting a programmable array with a different type of IC)." *Id.* at 42.

The record does not support this line of argument. The '035 patent also states "the use of the through-die area array contacts 70 . . . . *is not known to be possible* with any other currently available stacking techniques *since they all require the stacking contacts to be located on the periphery of the die*." Ex. 1001, 5:13–20 (emphasis added). This disclosure and others (including the disclosure of speed and bandwidth gains, reduced power and signal strength based on short via connections (*id.* at 4:62–67)) suggests that through-vias throughout the dies (as opposed to merely on the periphery) is a concept central to the disclosed and claimed invention. Moreover, the '035 patent provides a low level of detail in block form relating to connecting some contact points together for these alleged "use cases," further supporting the finding that the central focus of the invention was the large number of vias throughout the dies and implying that artisans of ordinary skill already knew how to connect circuits together (in parallel or otherwise) regardless of the types of circuits number of contacts involved. *See, e.g.*, Ex. 1001, Fig. 4, Fig. 5; Ex. 1002 ¶ 98 (discussing Figures 4 and 5), ¶¶ 235–236 (describing known implementations of parallel processing using stacked dies and testifying that "[b]eing able to do that in one massive shot over the image or set of frames in parallel would have been recognized as an advantageous way to apply Akasaka's teaching to the Zavracky-Chiricescu combination" (citing Ex. 1048 (Villasenor); Ex. 1021 (Koyanagi)), ¶ 332 (describing stacked structures with numerous vias throughout the dies as

"ubiquitous in the prior art" (citing Ex. 1020, 9–10; Ex. 1021, Fig. 4, 17; Ex. 1028, Fig. 9).

And as Petitioner persuasively explains, bus connections between a programmable array, memory, and a processor in these "use cases" were

> already taught in at least Zavracky (programmable array interconnected to memory and processor) and Chiricescu (programmable array interconnected to memory), and the teaching and advantages of a large number of interconnections between dies was well known. *See, e.g.,* Ex. 1009 (Alexander with large number of vertical interconnections between programmable array dies), Ex. 1021 (Koyanagi with large number of vertical interconnections between processor and memory dies), Ex. 1020, 2–10 (survey paper by Dr. Franzon describing general applicability and advantages of "area interconnection" with table listing "companies which provide area interconnection between stacked [chips]").

Reply 21.

Also, based on the above discussion, Petitioner does not rely on "merely disclosing the availability of large numbers of vertical interconnections between IC dies," as set forth above. *See* PO Resp. 41. As another example, Petitioner relies on Zavracky's teaching of "interconnection pads [for signals to] run in a vertical direction (the third dimension) between functional blocks" (Ex. 1003, 2:43–52) and descriptions involving Figures 12 and 13, which show similar buses connecting memory, FPGA, and a microprocessor. *See* Reply Br. 10; *supra* § II.D.4.

> Patent Owner also argues that
>
> > Petitioner provides no argument, let alone evidence, demonstrating that modifying the combination of Zavracky and Chiricescu to provide the type of wide configuration data port responsible for the accelerating features of the challenged claims (or to arrange a microprocessor and programmable array such that the two components share data) was either known in the art or within the skill of a POSITA.

PO Resp. 32. This argument repackages arguments, including unavailing claim construction arguments, addressed above in connection with claim 1 and below in connection with 23–25. *See supra* § II.D.4; *infra* §§ 6, 8. Other than numerous via connections, none of the challenged claims here recite or require other structure of a WCDP. Sharing data between a microprocessor and programmable array was well within the knowledge of an artisan of ordinary skill (as, for example, admitted for in connection with prior art Figure 1 of the '035 patent as discussed in connection with claims 9 and 25 above and as disclosed in Zavracky's Figure 13). Petitioner shows that implementing a WCDP in the context of the challenged claims, which Figure 5 of the '035 simply depicts as a black box, at most involves connecting large numbers of vias to connect circuits on stacked dies, and that such a scheme provides for parallel processing for different types of well-known circuits, all of which also was well-known and taught by the prior art of record. *See supra* § II.D.4, *infra* §§ 6, 8; Reply 9 (discussing a WCDP versus a narrow configuration port).

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 1–22, 36, and 38 would have been obvious.

6. *Claims 23 and 33*

Claims 23 and 33 are similar to claim 1, with the added limitations, "wherein said memory array is functional to accelerate external memory references to said processing element." Similar to the "programmable array" of claim 1, the "processing element" of claims 23 and 33, is a "field programmable gate array" (FPGA). Petitioner relies on its showing with respect to claim 23 to address claim 33. *See* Pet. 52–53.

Petitioner relies its showing with respect to claim 1, including relying on Zavracky's programmable logic array 802 as the claimed FPGA and random access memory 808 as the claimed memory array. *See* Pet. 44–47, 52–53. Petitioner also relies on the combined teachings of Zavracky and Chiricescu: "Chiricescu describes a system where the focus of the 3D module is on a FPGA layer and a memory layer designed to accelerate external references (and specifically, the reconfiguration data) to the FPGA layer (a programmable array), again providing a programmable array module." *Id.* at 45 (citing Ex. 1004 at II-234; Ex. 1002 ¶¶ 282–288). Petitioner also relies partly on its showings above with respect to the second integrated circuit in limitations [1.2] and [1.4], to include Zavracky's memory array stacked and electrically coupled to the first IC programmable

array, connected via multiple connection points. *See id.* at 24–25 (addressing limitation [1.2] relying on vertical buses, stacking, via holes, etc.), 28 (addressing limitation [1.4], which refers to limitation [1.3], collectively relying on multiple via connections including an array of contacts to provide vertical connections), 45 (referring to the analyses of limitation [1.2] and claim 2). For example, with respect to claim 2, Petitioner contends that "Chiricescu literally describes Zavracky as teaching technology 'to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.'" *Id.* at 30 (quoting Ex. 1004, II-232; reproducing Ex. 1003, Fig. 13, which shows multiple via bus layers).

In addition to the multiple short through-vias, Petitioner also relies on Chiricescu's RAM "cache memory" array teachings to show that on-chip memory (chips or layers in the same 3-D stack) accelerates configuration times relative to off-chip (chips or layers not in the same stack):

> The Zavracky-Chiricescu-Akasaka Combination provides this element. Chiricescu observes that "[t]he main bottleneck in the implementation of a high performance configurable computing machine is the high configuration time of an FPGA." Ex. 1004 at II-232; Ex. 1002, ¶¶304–07. This bottlenecking problem is caused in part by having to load configuration data from off-chip memory. Chiricescu's proposed solution used a "memory layer" where the "random access memory is provided to store configuration information." Ex. 1004 at II-232. Rather than having to go "off-chip" each time new FPGA

> reconfiguration data is referenced, Chiricescu's random access memory (i.e., a memory array) acts as a "cache memory" for that reconfiguration data, accelerating the FPGA (processing element)'s access to those external memory references. Ex. 1004, II-234. Therefore, the Zavracky-Chiricescu-Akasaka Combination, which includes Chiricescu's FPGA and memory layers, provides this claim element. Ex. 1002 ¶¶304–07.

Pet. 46–47. Petitioner also relies on "the Zavracky-Chiricescu-Akasaka Combination, which includes Chiricescu's FPGA and memory layers." *Id.* at 47 (citing Ex. 1002 ¶¶ 304–307). As summarized above in connection with claim 1, Petitioner relies on the knowledge of the artisan of ordinary skill and provides several reasons for combining the references to arrive at stacked chips with short via connections, for example, to increase processing speed based on shorter connections (decreasing propagation delays), increase bandwidth, and to increase processing based on parallel processing—thereby meeting the "functional to accelerate" limitation. Pet. 7–12, 16–20.

Addressing claims 23 and 33 as a group, Patent Owner contends that "[t]he Zavracky-Chiricescu-Akasaka combination fails to teach or suggest a 3-D processor module that includes a second integrated die element, separate from a first integrated die element having a programmable array, including a 'memory array is functional to accelerate external memory references to said processing element.'" PO Resp. 19. According to Patent Owner, "*Chiricescu* suffers precisely the same problems as the prior art distinguished in the '035 Patent," because

Chiricescu's' "narrow configuration data port still loads configuration data 'in a byte serial fashion and must configure the cells sequentially.'" *Id.* at 21 (quoting Ex. 1001, 3:66–4:1; citing Ex. 2011 ¶ 57). Patent Owner also argues that the "claims require" a "wide configuration data port." *Id.* at 20. Patent Owner also asserts that "as Dr. Franzon acknowledges, Chiricescu describes only a narrow configuration data port between the RLB [routing logic block] and memory layers." *Id.* at 21 (citing Ex. 2012, 80:10–22). Patent Owner also argues that "because Petitioner has not demonstrated that its combination of references 'accelerates external memory references to said processing element' over the baseline of the relatively narrow configuration port distinguished in the '035 Patent (and taught in Chiricescu), Petitioner's argument fails." *Id.* at 22 (citing Ex. 1001, 1:44–49, 4:42–47; Ex. 2011 ¶ 58). Patent Owner also indicates the claims require "utilizing a portion of the memory array as a wide configuration data port including buffer cells." *Id.* (citing Ex. 1001, 4:47–52).

These arguments do not undermine or address Petitioner's specific showing. Regarding separate wafers or dies, the Petition quotes Zavracky as disclosing "dies" and "individual dies," and persuasively argues that "[b]y the references to interconnected circuit elements or dies, the POSITA would have understood Zavracky to be describing stacked layers of integrated circuit die elements and depicting these in Fig. 13 and other figures." Pet. 22 (quoting Ex. 1003, 4:63–65; citing *id.* at Fig. 6, Ex. 1002 ¶¶ 278–280).

Regarding the WCDP claim construction arguments, apart from numerous via connections as set forth in our claim construction (*supra* § II.C), the challenged claims do not require other structure of a WCDP or buffer cells under our claim construction, and the specification does not describe the WCDP (depicted as black box) in Figure 5 as part of a memory array. *See supra* § II.C; Ex. 1001, Fig. 5. As Petitioner persuasively argues and as summarized above, the Petition relies on the combined teachings of Zavracky, Chiricescu, and Akasaka to teach the "functional to accelerate clause," and this combination is wider than a narrow port or any baseline. *See* Reply 4–9. As Petitioner also persuasively argues, even if the claims require a WCDP, according to Patent Owner's expert in the IPR2020-01020, IPR2020-01021, and IPR2020-01022, a "**configuration data port** . . . is . . . just a **data port used for configuration** . . . And **data port is just an interface to send data** from one place to another." *Id.* at 9 (quoting Ex. 1075, 163:8–163:21). "And 'the reason it's a very wide configuration data port is because it has a **lot of connections** through these TSVs between the memory die and the FPGA die.'" *Id.* (quoting Ex. 1075, 157:23–158:3). In other words, under Petitioner's persuasive showing, even if the claims require a WCDP, the combined teachings meet the challenged claims for the reasons noted.

Petitioner also persuasively shows that Patent Owner "misrepresents Dr. Franzon's testimony" regarding an alleged narrow port in Chiricescu. *See* Reply 11. As Petitioner persuasively argues, "Dr. Franzon's cited testimony: (1) has nothing to do with Chiricescu; (2) was given in response to a question about Trimberger; and (3) was discussing the

connection to "an **off-chip** memory" *Id.* (citing Ex. 2012, 80:10–22).

Dr. Franzon's cited deposition testimony supports Petitioner. Dr. Franzon's cited deposition testimony refers to Trimberger in the context of "off-chip memory that loads in through the data port," and Dr. Franzon testifies "a POSITA would interpret figure 5 [of the '035 patent] as [including an undepicted] similar narrow structure on the left of the very wide configuration data port" to load data from an external source. *See* Ex. 2012, 80:3–22. In other words, Dr. Franzon's testimony does not describe Chiricescu's stacked memory layer as using a *narrow* port to transfer reconfiguration data to the RLB (with FPGA gates) layer from an "on-chip" memory within the 3-D stack. *See* Ex. 1004, Fig. 2; *supra*

§ II.D.2.

Even if claims 23 and 33 require the capability to process data in parallel through the "functional to accelerate" limitations, as it shows for claim 1 (§ II.D.4), Petitioner persuasively shows that the Zavracky- Chiricescu-Akasaka 3-D module uses numerous vias throughout the dies to transfer data *between* the dies—i.e., acting to accelerate all manner of data and signals in parallel. *See, e.g.*, Pet. 16 (showing that Akasaka teaches that "'tens of thousands of via holes' permit parallel processing by utilizing the many interconnections,"; "as a result of this parallel processing, 'the signal processing speed of the system will be greatly improved'"; and "[d]ue to 'shorter interconnection delay time' arising from stacking and 'parallel processing' made possible from the area-wide interconnects, Akasaka states that 'twice the operating speed is possible in the best case

of 3D ICs' as compared to conventional designs" (quoting Ex. 1005, 1705)), 19 (arguing that "it was a predictable advantage and also suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity" (citing Ex. 1002 ¶ 233; Ex. 1005, 1705)).

As Petitioner also argues, Patent Owner's "'narrow data port' arguments are contrary to Chiricescu's teachings" and do not address the combined teachings of Chiricescu, Zavracky, and Akasaka. Reply 12 (citing PO Resp. 20–21). Petitioner notes that Zavracky, which Chiricescu references, describes "interconnects as being '*placed anywhere on the chip*' without restriction." *Id.* (quoting Ex. 1004, 232 (emphasis added). In addition, Petitioner notes that Chiricescu "discloses 'three separate layers with metal interconnects [including a "memory layer"] between them.'" *Id.* (quoting Ex. 1004, 232) (addition by Petitioner) (emphasis omitted). Vias running everywhere throughout the different stacked layers or dies as Zavracky, Chiricescu, and Akasaka individually and collectively teach distinguish over any alleged narrow port, and Petitioner provides well-known reasons for employing wide data ports, such as allowing for increased bandwidth and parallelism. *See* Pet. 7–12, 16–20; Ex. 1001, 5:16– 21 (describing "through-die array contacts 70 . . . routed up and down the stack in three dimensions" as "not known to be possible with any other currently available stacking techniques *since they all require the stacking contacts to be located on the periphery of the die*," so that by placing contacts throughout, "*cells that may be accessed within a specified time period is increased*").

Patent Owner also argues that "[b]ecause Petitioner does not allege that any 'external memory references' occur in *Chiricescu* (let alone that such references are accelerated), Petitioner cannot have met its burden to establish that Claims 23, 24, and 33 are obvious." PO Resp. 23.[21] According to Patent Owner, "Petitioner misinterprets the term 'external memory references,' suggesting that this term too can be satisfied simply by storing a certain type of data in Chiricescu's memory." *Id.* (citing Pet. 47; Ex. 1002 ¶ 47). Patent Owner also argues that "memory references are not data, but are instructions directed to a particular place memory address [sic] in memory." *Id.* (citing Ex. 2011 ¶ 60; Ex. 2015, 181; Ex. 2012, 49:11– 50:1). Dr. Souri's cited declaration testimony does not tie his opinion that "[a] skilled artisan understands that memory references are not data" to claims 1, 5, 10, 16, and 23 as viewed in light of the '035 patent specification. *See* Ex. 2011 ¶ 60.

In addition to citing Dr. Franzon's deposition testimony, which does not support Dr. Souri as indicated above, Dr. Souri cites "Ex. 2015 at 181." This particular extrinsic evidence, which includes a single page out of what appears to be a text book, is not helpful because it does not have anything to do with accelerating memory references, and it describes types of "operands," which are not at issue in the '035 patent. Ex. 2015, 181 ("The third type of operand is a memory reference."). In other words, Dr. Souri's testimony is conclusory as it does not address how this extrinsic evidence relates to the recited "functional to accelerate external memory references" clause as

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[21] Claim 24 depends from independent claim 23. We address claim 24 below. *See infra* § III.D.7.

recited in claim 23 and in the context of the cache memory or reconfiguration scheme as set forth in the '035 patent specification. *See* Ex. 2011 ¶ 60 (citing Ex. 2015, 181). Patent Owner and Dr. Souri also do not explain clearly how the cited deposition of Dr. Franzon supports Patent Owner. *See* PO Resp. 23 (citing Ex. 2012, 49:11–50:1; Ex. 2011 ¶ 60); Ex. 2012, 49:11–50:1 (generally testifying that "Chiricescu's FPGA processing element" is "agnostic" as "to what actually is stored in it").

Petitioner persuasively shows that caching external memory references in a stacked cache memory satisfies the "functional to accelerate" limitations relative to loading them from off-chip (outside of the stack), at least because of "caching" *and* "the use of short electrical paths, or significantly increased number of connections" including "Akasaka's area- wide distributed interconnects." *See* Reply 8 (citing Pet. 13–31, 44–47); *see also id.* at 13 (discussing hitting the cache with external memory references (citing Ex. 1002 ¶¶ 215–216; Ex. 2012, 42:9:14, 48:6–50:1).

Petitioner also persuasively explains that even under Patent Owner's narrow reading of "external memory references," as related to memory addresses, Chiricescu teaches it because the memory address references will "hit" the cache. *See* Reply 12–13 (citing Ex. 1002 ¶¶ 215–216). Supporting Petitioner, Dr. Franzon persuasively testifies at the cited paragraphs of his declaration as follows:

> 215. . . . The POSITA would recognize that what Chiricescu is teaching is to use that memory as a "cache" . . . . By doing so, the FPGA's external memory references . . . will be accelerated

> because [they] will "hit" in the "cache" and be returned from the on-chip memory without having to go off-chip.
>
> 216. Chiricescu is thus teaching to the POSITA to accelerate memory lookups that are directed to the external chip by sending them instead to the on-chip memory, perhaps keeping a relevant set of data to the application. This is what Chiricescu means when it says that "a management scheme similar to one used to manage cache memory can be used to administer the configuration data."

Ex. 1002 ¶¶ 215–216; Reply 13 (quoting part of the same two paragraphs).

As Petitioner also persuasively argues, the '035 patent does not limit "external memory references" in particular, but it does refer to cache memory and enhancing reconfiguration speed with such memory. *See* Reply 13 (citing Ex. 1001, 2:11, 2:25, 4:31, 4:57–58); Ex. 1001, 4:31–36 (referring to "cache memory 66" as serving its "traditional role of fast access memory," and also including accessing by "both the microprocessor 64 and FPGA 68 with equal speed," in the context of "reconfigurable computing systems").

Patent Owner also argues that "[b]ecause the claims require a '***memory array*** is functional to accelerate external memory references to said processing element,' Petitioner's focus on the type of data stored in the array misses the mark." PO Resp. 22. Contrary to this argument, as discussed above, Petitioner relies on a cache memory array as combined in a 3-D stack with short via connections, not the type of data. As discussed throughout this Final Written Decision, the Petition persuasively

relies on such short and numerous distributed vias as structure for the "functional to accelerate" clauses, because such structure provides shorter path delays and allows for increased bandwidth and parallel data transfer. *See supra* §§ II.D.3 (Akasaka's parallel processing and multiple via teachings), II.D.4– 5 (analyzing claim 1 motivation (which applies here) as Petitioner shows as including, *inter alia*, increased bandwidth, parallel processing, and decreasing path delays); Pet. 8–12 (background knowledge of an artisan of ordinary skill includes stacking chips with multiple distributed vias to minimize latency and maximize bandwidth), 16–20 (similar, listing multiple reasons to combine Zavracky, Chiricescu, Akasaka, including to accelerate data via shorter interconnection delay times, parallel processing, increased operating speed, etc.). Essentially, the cache memory relied upon by Petitioner carries all of these advantages, because it is within the 3-D stack instead of "off-chip."

In the Sur-reply, Patent Owner argues that "[t]he entire point of Chiricescu is that it achieves accelerated FPGA configuration by storing configuration data 'on-chip' so that it does not need to load configuration data from off-chip." Sur-reply 5. Patent Owner also argues that "all off- chip connections are carried out through a typical narrow configuration data port, that suffers the same problems as the prior art distinguished in the '035 Patent." *Id.* Patent Owner then argues that "moving *Chiricescu's* cache memory off-chip (i.e., into *Zavracky's* 3D stacked memory die) eliminates the benefit gained from moving the memory on-chip, [so] a POSITA would not have contradicted *Chiricescu's*

fundamental teachings to arrive at Petitioner's proposed combination." *Id.* at 5–6.

These arguments mischaracterize Petitioner's showing and confuse the issues as discussed in the previous section. *See supra* § II.D.5; note 19. Patent Owner essentially conflates narrow ports having large signal delays over long electrical planar paths with "all off-chip connections" as applying to Zavracky's 3-D stack (by referring to each separate chip in Zavracky's modified 3-D stack as "off-chip" and ignoring the central fact that each chip connects to the other chips by numerous short vias). There is no support for this line of argument. Moreover, "Dr Franzon not[ed] the routine use of on- chip area-wide connections in 3D stacks, including his prior work." Reply 18 (citing Ex. 1002 ¶¶47–51; Ex. 1070 ¶¶ 65; Ex. 1020; *see also* Ex. 1004, Fig. 2, II-232 § 1 (describing "on chip random access memory . . . provided to store configuration memory"—i.e., the memory layer of Figure 2); *supra* note 19. Patent Owner agrees that Chiricescu discloses "on-chip cache memory" as a separate layer in a chip, which further suggests a separate memory layer in a stack of dies. *See* Sur-reply 5.

Nevertheless, Patent Owner contends that "the movement of *Chiricescu's* on-chip cache memory to *Zavracky's* off-chip memory would throttle" speed gains. Sur-reply 5. For the reasons explained above, this line of argument confuses issues and mischaracterizes Petitioner's showing. *See supra* note 19. Chiricescu's teachings bolster Zavracky's FPGA teachings, and Petitioner shows that in this context, Zavracky describes a memory layer, microprocessor layer, and FPGA layer in a 3-D stack with each layer

or chip connected by numerous short vias to increase speed. *See, e.g.*, Pet. 14–15; Ex. 1003, Fig. 13. Patent Owner's attempt to conflate all "off- chip" narrow port disadvantages to Zavracky's modified stack of chips by calling that stack "off-chip" is unsupported. *See* Sur-reply 5. As Petitioner persuasively shows throughout its briefing, Zavracky's stack of chips, connected by numerous vias, and bolstered by Akasaka's numerous via and Chiricescu's FPGA teachings, operates just like Chiricescu's "on-chip" circuit layers in a single chip connected by numerous vias in terms of speed and acceleration. *See* Reply 6–7 ("Zavracky's short interior 'inter-layer connectors' to stacked 'random access memory . . . results in **reduced** memory access **time**, **increasing the speed** of the entire system,'" and "Chiricescu also teaches the **acceleration** advantages and 'significantly **improve[d FPGA] reconfiguration time'** achieved by its interconnected layers, including a memory layer configured as a cache for fast access to 'configuration data . . . from memory off-chip.'" (quoting Ex. 1003, 11:63– 12:2; Ex. 1004, 23[4])), 7 (noting Akasaka's "**acceleration** advantages" based on "teaching, e.g., that '[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing' and that 'shortening of interconnections and signal transfer through vertical via holes in the 3-D configuration provides advantages for the design of large-scale systems.'" (quoting Ex. 1005, 1705)). In other words, as Petitioner shows, in addition to "stacking techniques," "[t]he Zavracky-Chiricescu-Akasaka Combination also discloses the other ways that the '035 patent even arguably implies increases speed—i.e., through caching, the use of short electrical paths, or significantly increased number of

connections." *Id.* at 8 (citing Pet. 13–31, 44–47); Ex. 1070 ¶ 44 ("[A] POSITA would have recognized that [a] 3D chip that consists of multiple dies would do a better job than the 2D chip and provid[e] fast large connectivity. . . . The point here is that a shorter vertical interconnect allows for a shorter 'longest path' and a faster chip.).

Petitioner also persuasively addresses Patent Owner's argument that the claims require acceleration over a "baseline" and other related arguments. *See* PO Resp. 20–21; Reply 12 (persuasively arguing that the combined teachings contribute to acceleration, the combination does not include a "narrow port," and "Dr. Franzon testified in both his declaration and deposition that the Zavracky-Chiricescu-Akasaka combination provides acceleration compared to the baseline of other prior art with different structural characteristics." (citing Ex. 1002 ¶¶ 212, 215–17, 304–05; Ex. 2012, 28:9–21, 28:9–21, 29:15–33:15)); *see also supra* §§ II.C (claim construction); II.D.1 (discussing claim construction and analysis of claim 1 in relation to prior art Figure 3's 8-bit narrow port—i.e., one type of baseline). Zavracky indicates that 32 bit microprocessors were routine in 1993, years before the effective date of the invention, indicating that Zavracky's microprocessor buses at least handled 32 bits in parallel. *See* Ex. 1003, 1:6–8 (continuity date of 1993), 1:31–40 (discussing prior art microprocessors). As noted above, Patent Owner indicated during the Oral Hearing that the challenged claims embrace devices transfer data over a port that "could be as small as 32 bits . . . if you have a small FPGA, right? If you want to update something in parallel, you could update 32-

bit with 32 bits?" Tr. 49:1–9; *supra* § II.C (claim construction).

Addressing claims 23, 30, and 33 together, Patent Owner argues that "major modifications would need to be made to the combination of *Zavracky* and *Chiricescu* in order to configure a stacked module to meet the acceleration limitations of Independent Claims 23, 30, and 33." PO Resp. 31. Patent Owner explains that this major modification requires a "wide configuration data port (or other similar structure) between the memory and the FPGA." *Id.* Patent Owner also argues that such a modification would "alter *Chiricescu's* principle operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB Bus and its 'routing layer,' which *Chiricescu* declares '***is of critical importance*** since it is used for the implementation of the interconnection of the non-neighboring RLBs.'" *Id.* at 31–32 (quoting Ex. 1004, 2) (emphasis by Patent Owner).

Here, Patent Owner concedes that "the '035 Patent discloses a memory array that achieves the claimed acceleration (*i.e.*, utilizing a *portion of the wide configuration data port*), which significantly reduces the amount of time it takes to move data from a memory die into a programmable array." PO Resp. 32 (emphasis added). Patent Owner does not describe what "portion" of the WCDP (which Figure 5 of the '035 patent depicts as a black box) that the claimed "functional to accelerate" limitations require. In any event, as Petitioner argues and as adopted as our claim construction above, the '035 patent shows that "functional to accelerate" limitations include "a number of vertical contacts distributed throughout

the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory array and processing element." *See supra* § II.C (claim construction). For the reasons explained above in connection with claim 1 and within this section, the combined teachings of Zavracky, Chiricescu, and Akasaka satisfy the "functional to accelerate" limitation of claim 23. *See supra* II.D.4–5.

With respect to Chiricescu's principle of operation, as Petitioner also persuasively argues, no "'modifications' are required to Chiricescu at all because the Petition's combination involves 'fold[ing] in Chiricescu's teachings (including using stacked memory to reconfigure[] the FPGA) with Zavracky's 3D stacks." Reply 17–18 (quoting Pet. 17). Even if employing Chiricescu's FPGA structure also suggests implementing its routing layer on a separate layer, contrary to Patent Owner's arguments, Chiricescu does not describe its routing layer as a narrow port, as also explained within the instant section above. *See id.* at 18 (noting that Dr. Franzon did not admit Chiricescu includes a narrow port and citing Dr. Franzon's testimony that on-chip area-wide connections in 3-D stacks were well-known (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68)). Also, Chiricescu's Figure 2 depicts connections between the memory layer, routing layer, and RLB layer (a "sea-of-gates FGPA structure") with connections that are distinct from the RLB bus. Ex. 1004, II-232 § 2.1, Fig. 2. Chiricescu notes that "routing congestion will also be improved by the separation of layers," further suggesting that vias connected throughout including to the routing layer is not a narrow port. *Id.* at II-232.

As Petitioner persuasively argues, "Chiricescu describes 'vertical metal interconnections (i.e., interlayer vias),' and '**three separate layers with metal interconnects between them**.'" Reply 16 (citing Ex. 1004, II- 232). Also, Chiricescu's "express 'architecture is based on' technology developed by Zavracky at Northeastern University." *Id.* (quoting Ex. 1004, II-232). And Chiricescu states that Zavracky's architecture provides "3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) *placed anywhere* on the chip." Ex. 1004, II-232 (emphasis added). Therefore, contrary to Patent Owner's arguments, Chiricescu's principle of operation does not require a narrow port. *See also* Reply 16 ("The combination involves 'fold[ing] in Chiricescu's teachings (including using stacked memory to reconfigure the FPGA) with Zavracky's 3D stacks.'" (citing Pet. 17)). Moreover, increasing via connections based further on Akasaka's teachings would have been obvious by facilitating more connections between well-known available circuits such as memory, FPGA, and processors. *See, e.g.*, Reply 19 ("Zavracky and Chiricescu envision connections 'anywhere on the die.'" (citing Pet. 14–15; Ex. 1002 ¶¶ 41–51, 237–238)); Pet. 20 ("Akasaka's distributed contact points would have been the logical extension to Zavracky and Chiricescu's teaching of connections anywhere, especially in view of the POSITA's background knowledge." (citing Ex. 1002 ¶ 239)).

Accordingly, Patent Owner's arguments alleging "major modifications . . . in the combination of *Zavracky* and *Chiricescu* in order to configure a stacked module to meet the acceleration limitations of Independent Claims 23, 30, and 33," related

arguments including the "principle [of] operation" of Chiricescu, and claim construction arguments, as summarized above, are unavailing.

We adopt and incorporate Petitioner's showing as to claims 23 and 33, as set forth by the Petition and summarized above, as our own. *See* Pet. 7– 20, 44–47, 52–53. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 23 and 33 would have been obvious.

7. *Claims 24 and 30*

Claim 24 depends from claim 23 and recites "[t]he programmable array module of claim 23 wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element." Petitioner contends that "[t]he 'external memory references' analyzed in [23] comprise reconfiguration data, thereby providing this claim. Chiricescu describes that the accelerated reconfiguration data is used to reconfigure the FPGA as a processing element." Pet. 47 (citing Ex. 1004, II-234 (describing "when the FPGA is reconfigured from performing A x B to A x C or vice versa."); Ex. 1002 ¶¶ 304–07). Independent claim 30 is materially similar to dependent claim 24 (both reciting, *inter alia*, "wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element"). Petitioner refers to its showing of independent claims 1 and 23 and dependent claim 24 to address claim 30. *Id.* at 51–52.

In other words, as discussed in the previous section addressing claims 23 and 33, Petitioner persuasively shows that the combined teachings accelerate external memory references (which include reconfiguration data) to the FPGA processing element, showing that the "memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element."

Addressing claims 24, 30, and 32 as a group, Patent Owner argues that "[t]he *Zavracky-Chiricescu-Akasaka* combination fails to teach or suggest a 3-D processor module that includes a second integrated die element, separate from a first integrated die element having a programmable array, wherein the 'memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.'" PO Resp. 23–24.[22] Patent Owner recites the "functional to accelerate memory references" and "functional to accelerate reconfiguration" clauses, points to Petitioner's "same rationale" with respect to claims 23 and 33 discussed in the previous section (§ II.D.5), and concludes that claims 24, 30, and 32 "are therefore patentable." *Id.* at 24 (noting that "Petitioner relies on the same rationale for this claim element as it did for the element discussed directly above, i.e. 'memory array is functional to accelerate external memory references to said processing element'"). Patent Owner's arguments with respect to claims 24, 30, and 32 as outlined herein do not undermine Petitioner's

[22] The analysis of claim 32 is below. Claim 32 depends from claim 31, and Petitioner contends that the combination of Zavracky, Chiricescu, Akasaka, and Trimberger would have rendered claims 31, 32, and 34 above. *See infra* § II.E.2.

persuasive showing as summarized above including for the reasons discussed above in connection with claims 23 and 33. *See* Pet. 46– 47, 51–52; *supra* § II.D.6.

We adopt and incorporate Petitioner's showing as to claims 24 and 30, as set forth by the Petition and summarized above, as our own. *See* Pet. 7– 20, 47, 51. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 24 and 30 would have been obvious.

8. *Claims 25–29*

Like independent claim 17, independent claim 25 tracks the limitations of claim 1, and recites at least three die elements (instead of at least two as in claim 1), with the three die elements including a programmable array, processor, and memory electrically coupled together as in claim 17. *See supra* § II.D.4 (analyzing claims 1 and 17). Claim 25 also recites "whereby said processor and said programmable array are operational to share data therebetween."

Addressing claim 25, Petitioner relies on its showing for claims 1 and 17, including Zavracky's disclosure of programmable logic array 802 in a stacked 3-D processor module with microprocessor layers 804 and 806 as Figure 13 depicts, and Chiricescu's teaching of a 3-D chip comprising FPGA, memory, and routing layers. *See* Pet. 21–29, 41–43, 47–50. Petitioner also asserts that with respect to

Zavracky's Figure 13, "each of the programmable array, microprocessor, and memory are pair-wise stacked with and electrically coupled with each other." *Id.* at 25. Petitioner also relies Akasaka's teachings and on similar motivation as for claims 1 and 17. *See id.* at 17–20, 49–50 ("As discussed, §VII.A.4, a POSITA would have been motivated to employ Akasaka's thousands of via holes in the context of Zavracky." (citing Ex. 1002 ¶¶ 233–39, 347–48; Pet. § VII.A.4)).

Addressing the claim 25 limitation "whereby said processor and said programmable array are operational to share data therebetween," Petitioner relies partly on Akasaka's disclosure of 3-D chips wherein "memory data are kept common by the interlayer (vertical) signal [so that] **each processor can use the common memory data**." Pet. 49 (emphasis by Petitioner) (quoting Ex. 1005, 1713). In addition, Petitioner argues that "the POSITA knew of the need for replicated 'common data memory' in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence." *Id.* at 19–20 (citing Ex. 1002 ¶ 236; Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25). Petitioner further explains that "[t]hat structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky," further motivating "[a] POSITA . . . to seek out Akasaka's distributed contact points in order to build a 'common data memory.'" *Id.* at 20 (citing Ex. 1002 ¶ 237).

Petitioner also relies on Akasaka's teaching that that "information signals can be transferred" through "several thousands or tens of thousands of via holes . . . present in these devices" to further suggest

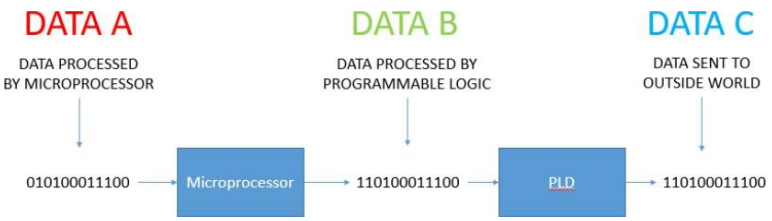
employing Akasaka's "thousands of via holes in the context of Zavracky" as further suggesting the claimed data sharing feature. Pet. 49–50 (first two quotes quoting Ex. 1005, 1705; citing Ex. 1002 ¶¶ 233–239, 347–348). As noted throughout this Final Written Decision, Petitioner also relies on known benefits of increased speed, bandwidth, and capability for parallel processing based on well-known teachings, to suggest stacking layers, including memory layers, using numerous vias, to combine the teachings of Zavracky, Chiricescu, and Akasaka. *See id.* at 8–9, 16–20.

Petitioner explains that Zavracky also teaches that its programmable logic 802 is an FPGA and serves as "an intermediary between 'the microprocessor and any off-chip resources.'" Pet. 48–49 (citing Ex. 1003, 12:28–36). Petitioner also relies on Zavracky's "[i]nterconnect lines" operating as a "data bus." *Id.* at 49 (quoting Ex. 1003, 6:39–42). According to Petitioner, a "POSITA would have recognized that communication between 'the microprocessor and any off-chip resources' via the FPGA (under the Zavracky-Chiricescu-Akasaka Combination as explained in [1.1], [1.2] and [2]) means that data is shared between the microprocessor and the FPGA." *Id.* (citing Ex. 1002 ¶ 342).

Claims 26–29 depend from independent claim 25. Claim 26 recites "wherein said memory is operational to at least temporarily store said data." *See* Pet. 50. Petitioner argues that "[t]he POSITA would have understood that memory is—by definition—operational to at least temporarily store data." *Id.* (citing Ex. 1002 ¶ 308 (citing Ex. 1039 (trade dictionary defining memory)). Petitioner also relies on

Akasaka's shared memory as discussed above and further below in connection with claim 25. *See id.* at 47–50 (citing Ex. 1005, 1713). Petitioner asserts that the added claim limitations of claims 27–29, which recite an "FPGA," a "microprocessor," and a "memory array," respectively, read on Zavracky's stack as depicted in Figure 13. *See id.* at 50–51 (relying on the analysis for claims 18–20, which in turn rely on the analysis for claims 1 and 3–6 (*see id.* at 43)).

Patent Owner groups claims 25–29 together and argues that "[t]he *Zavracky* microprocessor and programmable logic are not operational to ***share*** data, such as might be stored in a stacked memory die, for example." PO Resp. 25 (citing Ex. 2011 ¶ 63). Patent Owner reproduces the following diagram from Dr. Souri's declaration to illustrate its point:



Ex. 1012 ¶ 63. According to Patent Owner, Zavracky's microprocessor on the left does not share data with the FPGA (PLD) on the right, because "it is the output of Zavracky's microprocessor that is sent to the FPGA." PO Resp. 25 (citing Ex. 1012 ¶ 63).

Patent Owner attempts to distinguish "sharing" data and "transferring" data by arguing that "[t]he claims require more than a processor transferring data to a field programmable." *See* PO Resp. 24–25. Neither the '035 patent specification nor claims 25–29 requires this distinction. Nevertheless, Patent Owner

argues that shared data "might be stored in *a stacked memory die*, for example." PO Resp. 25 (emphasis added). Patent Owner similarly argues in its Sur-reply that "[a] POSITA would recognize that this data *on the stacked memory die* is literally 'data shared between a microprocessor and an FPGA.'" Sur-reply 12 (citing Ex. 2011 ¶ 64; Ex. 1001, 1:59–67, 2:47–51, 4:31–36) (emphasis added).

Contrary to this line of argument, claims 25–29 do not require a "stacked memory die" to hold data to support the recited shared data functionality. Although claim 26 recites "wherein said memory is operational to at least temporarily store said data," claim 26 is broad enough to read on Zavracky's modified memory (which is operational to store the shared data) *after* the microprocessor and FPGA (are operational to) share it per claim 25. *See* Pet. 50 (arguing that "[t]he POSITA would have understood that memory is—by definition—operational to at least temporarily store data" (citing Ex. 1002 ¶ 308 (citing Ex. 1039 (trade dictionary defining memory)).[23]

Moreover, even under Dr. Souri's diagram of Zavracky's process, Zavracky's microprocessor processes the input data to create the shared output data, and then transfers that shared output data onto the data bus and then to the FPGA. *See* Reply 13–14 (citing Ex. 1070 ¶¶ 73–74; Ex. 1083); Ex. 1070 ¶ 73 (quoting Ex. 1083, 1:26–34 (describing computers "shar[ing] data" by "transfer[ing] data")); Pet. 49

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[23] As indicated herein, Patent Owner does not address Petitioner's persuasive showing for claim 26 separately from claim 25. Petitioner also persuasively relies on Akasaka's shared memory for claims 25–29 as discussed further below. *See* Pet. 47–50 (citing Ex. 1005, 1713).

(citing Ex. 1002 ¶¶ 342, 349). As discussed further below, Petitioner also persuasively explains how Zavracky's microprocessor and FPGA share and process the same data from off-chip resources to implement a user-defined protocol. *See* Pet. 48–49.

Patent Owner also argues that Petitioner's alternative theory based on Akasaka's teaching and suggestion to share "'common memory data' does not cure this fundamental deficiency in Zavracky because it also does not involve any processing of data shared between a microprocessor and an FPGA (or any other type of chip)." PO Resp. 26. Claims 18–22 do not require "processing of [shared] data," but even if the claims imply that interpretation, the combined teachings suggest it, as Petitioner persuasively shows as discussed next.

To support its point, Patent Owner reproduces Zavracky's Figure 25 as follows:

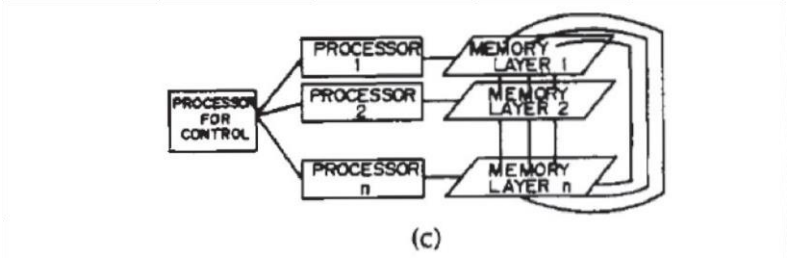

Fig. 25. New concept of 3-D IC. (a) 3-D PLA model (by Prof. T. Nanya of the Tokyo Institute of Technology). (b) Integration of CAM RAM in the same chip (by T. Ogura of NTT). (c) Common memory data system for 3-D memory chip (by Prof. M. Hirose of Hiroshima University).

PO Resp. 26. Figure 25(c) above depicts a "[c]ommon memory data system for a '3-D memory chip' wherein

processors 1, 2, n (on the left) share data on memory layers 1, 2, n (on the right)." Ex. 1005, 1713. Akasaka states that "memory in each chip belongs to corresponding independent microprocessors in the same layer, *and the memory data are kept common by the interlayer (vertical signal) transfer*." *Id.* (emphasis added).

Patent Owner argues that "although *Akasaka* proposes that memory data is 'kept common by the interlayer (vertical) signal transfer,' the individual microprocessors do not process any shared data because each only processes the data in its corresponding memory." PO Resp. 26–27. This argument misses the mark, because Akasaka's system transfers the same data between the memories so that each processor is operational to process the same data. Stated differently, Akasaka contradicts Patent Owner's argument that transferring the same data at one memory location (the "common" data in Akasaka) to another memory location shows a lack of data sharing—i.e., Akasaka describes the data as "common." *See* Ex. 1005, 1713.

As to sharing data between a processor and an FPGA, Petitioner relies on Akasaka's teaching as suggesting the sharing of common data through vertical data transfers in the combined 3-D structure of Zavracky, Chiricescu, and Akasaka, instead of relying on a bodily incorporation of the processor memory layer scheme of Akasaka. *See* Pet. 49–50; Reply 15 (arguing that Patent Owner "attacks the physical die-stacking technique in Akasaka—but Akasaka is not relied upon to teach die-stacking" and "Zavracky already teaches stacked memories that are interconnected to other dies in the stack, and also

teaches memories can be at any layer" (citing Ex. 1003, 11:63–12:2, Figs. 10, 12)). Claims 25–29 are agnostic as to how the FPGA and microprocessor share data—i.e., with or without a separate memory in each layer—i.e., claim 25 recites "whereby said processor and said programmable array are operational to share data therebetween" without reference to the "memory" recited earlier in the claim.

As proposed by Petitioner, it would have been obvious for the FPGA and microprocessor of Zavracky-Chiricescu, based on Akasaka's teachings, to share data using numerous (e.g., thousands) of vertical vias to implement the data transfer and thereby increase processing speeds and bandwidth. *See* Pet. 49–50 (citing Pet. § VII.A.4 (reasons to combine the references); Ex. 1002 ¶¶ 233–239; 347–348). For example, as Petitioner shows, using Akasaka's teaching to share data using thousands of vertical vias would have "increase[d] bandwidth and processing speed through better parallelism and increased connectivity." *See* Pet. 19 (§ VII.A.4), 49–50; Ex. 1005, 1705; Reply 6–7 (citing known advantages of numerous vertical vias). Petitioner persuasively shows that artisans of ordinary skill would have recognized that sharing common data by an FPGA and processor using the dense via structure of Akasaka increases processing speed and ensures cache coherency. *See* Pet. 19–20 (Ex. 1002 ¶¶ 236–237; Ex. 1005, 1705).

Patent Owner's arguments do not address Petitioner's more general showing that a "POSITA would have recognized that communication between 'the microprocessor and any off-chip resources' via the FPGA (under the Zavracky-Chiricescu-Akasaka

Combination as explained in [1.1], [1.2] and [2]) means that data is shared between [and processed by] the microprocessor and the FPGA." Pet. 49 (citing Ex. 1002 ¶¶ 342–44, 349). In other words, Dr. Souri's diagram above only refers to data *from* the PLD (FPGA) as "DATA SENT TO THE OUTSIDE WORLD," but this analysis does not address Petitioner's persuasive showing that data from the outside world (off-chip) sources passes through the FPGA as an intermediary to the microprocessor. *See* Pet. 48–49 (citing Ex. 1003, 12:28–36). At the cited passage, prior to describing Figure 13, Zavracky states that "[p]rogrammable logic arrays can be used to provide communication between a multi-layered microprocessor and the outside world." Ex. 1003, 12:29–31. Zavracky also states that "programmable logic array 802 [an FPGA in Figure 13] can be programmed to provide for user-defined communications protocol between the microprocessor and any off-chip resources." *Id.* at 12:36–37. Figure 13 shows bus connections on the PLD 802 (FPGA) to the outside world, with bus connections from PLD 802 to microprocessor 804/806 and memory 808. *See* Ex. 1003, Fig. 13, 12:29–39. Therefore, as Petitioner argues, Zavracky shows that communication occurs between the microprocessor and the FPGA, thereby teaching the sharing of data between the two (in at least one of the two directions). *See* Pet. 48–49.

In addition, in advancing another argument, Patent Owner admits that the combination teaches data sharing: "[T[he approach of Zavracky- Chiricescu would result in a structure in which *data is removed from the microprocessor cache and placed in the FPGA's on-chip memory*," and "*data . . . might be*

shared between *Chiricescu's* FPGA and *Zavracky's* microprocessor." PO Resp. 28–29 (emphasis added).

Further addressing claims 25–29 as a group, Patent Owner argues that "to modify the *Zavracky-Chiricescu* system with *Akasaka*, . . . the ***stacked*** memory layer of *Chiricescu* would need to be moved into its RLB layer because *Akasaka* requires each memory layer to be located on the same layer as its associated processor," thereby requiring a "major modification" of Chiricescu. PO Resp. 36–37. Patent Owner similarly argues that implementing the combination requires "adding ***more*** structure to *Chiricescu's* RLB layer, in the form of *Akasaka's* memory, destroys *Chiricescu's* principle of operation, which relies on moving as much structure ***out of*** the RLB layer as possible." *Id.* at 37.

This line of argument incorrectly assumes that Petitioner must show how to bodily incorporate the common memory teachings of Akasaka into Chiricescu's structure as part of its obviousness showing. This argument is unavailing, because Petitioner relies on Zavracky's 3-D stack structure, including its memory as a separate layer, as modified by the common memory teachings of Akasaka, without any modification to Chiricescu's FPGA teachings required. The common memory teachings of Akasaka are agnostic as to the memory location.

That is, Akasaka does not "require[] each memory layer to be located on the same layer as its associated processor." *See* PO Resp. 36. Even though Figure 25 of Akasaka shows a stack of processors and memory, with a processor and memory on the same layer, nothing in Akasaka states that the memory cannot be elsewhere in the stack on a separate layer. Rather,

Figure 25 shows all memories connected together electrically with each memory connected electrically to its respective processor. *See* Ex. 1005, Fig. 25. These electrical connections suggest to an artisan of ordinary skill that the memory layer's location is less important than the electrical connections. *See id.* Moreover, Petitioner relies on Zavracky's separate layer for each memory in a stack with via connections to enhance speed, as the combination suggests. *See* Reply 15 ("Zavracky already teaches stacked memories that are interconnected to other dies in the stack, and also teaches memories can be at any layer" (citing Ex. 1003, Figs. 10, 12, 11:63–12:2 ("[A]n additional layer or several layers of random access memory may be stacked. . . . This configuration results in reduced memory access time, increasing the speed of the whole system")).

Addressing 23–30 and 33–35 as a group, Patent Owner contends that "Petitioner's arguments for combining *Zavracky* and *Chiricescu* (*see* Petition at 18) also fail because they are untethered from the Challenged Claims and do not establish that it would have been obvious to 'combine[] these particular references to ***produce the claimed invention***.'" PO Resp. 29 (quoting *Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (emphasis by Patent Owner).).

Patent Owner argues that

> is insufficient to "accelerate external memory references to said processing element" or "accelerate reconfiguration of said field programmable gate array as a processing element," and Petitioner fails to articulate any reason that Chiricescu's alleged teaching of

> performing "arbitrary logic functions" is related to the claimed invention.

PO Resp. 30.

Contrary to these arguments, Petitioner provides persuasive reasons to provide numerous vias throughout the Zavracky's layers or dies based on the collective teachings of the references, showing that it was well-known that providing such vias allows for speed increases, increased bandwidths, parallel processing, and further allowing for accelerated external memory references and reconfiguration of an FPGA through the additional use of cache memory, as discussed above in connection with claims 1, 23–25, 30, and 33. *See supra* §§ II.D.4–7. Petitioner's Reply also summarizes Dr. Franzon's testimony showing that improving reconfiguration times by using the stacked memory techniques (including the distributed vias) as suggested by the combined references accelerates memory references. *See* Reply 16– 17 (citing Ex. 1002 ¶¶ 215–17, 221–230, 302–303).

Further addressing claims 23–30 and 33 as a group, Patent Owner contends that "Dr. Franzon admitted that a wide configuration data port that accelerates a programmable array's external memory references to a stacked memory die as compared with the slow narrow bus disclosed in Chiricescu was not obvious at the time of the invention." PO Resp. 33 (citing Ex. 2012, 71:19–72:1). Based on this characterization, Patent Owner also argues that "the wide configuration data port of the '035 Patent provides precisely the answer to what Dr. Franzon admits was practically impossible at the time of the invention." *Id.* (citing Ex. 2012, 71:19–72:1, 80:3–22; Ex. 2011 ¶ 73). Patent Owner adds that this

"skepticism of Petitioner's own expert demonstrates that the challenged claims are patentable." *Id.* (citing Ex. 2011¶ 73). Contrary to this line of argument, Dr. Franzon does not admit that a wide configuration data port was not obvious, and does not admit that Chiricescu discloses a narrow data bus. *See* Ex. 2012, 71:19– 72:1, 80:3–22. Rather, at the cited deposition testimony, Dr. Franzon testifies that "*off-chip* access can't be, for example, 100,000 bits wide." *Id.* at 71:21–23 (emphasis added). Here, in context, Dr. Franzon states that "you can't have that number of IO . . . . in [the] *case of Trimberger and the '226 patent* [which is related to the '951 patent, *see* IPR2020-01571] *memory going form the external to the module*." *Id.* at 71:23–72:1 (emphasis added). Here again, Patent Owner conflates a narrow data port from a source "external to the module" (i.e., external to the claimed 3-D stack), with a wide data port from a memory within the stack to other chips in the stack. *See supra* note 19.

Further grouping claims 23–30 and 33 together, Patent Owner argues that

> Petitioner has not produced a single reference or combination of references that teaches or suggests stacking a processor with a programmable array in a manner in which is operational to share data therebetween, or a memory array functional to accelerate external memory references or accelerate reconfiguration of FPGA.

PO Resp. 31. This line of argument repackages arguments addressed in this section and above in connection with claims 1, 9, 23–25. *See supra* §§ II.D.5–6, 8. As noted above, Petitioner relies on a

combination of references under obviousness to address the "functional to accelerate" clauses. As also discussed above, Zavracky's Figure 13 explicitly illustrates a stacked die structure with PLD 802 (FPGA), microprocessor 804/806, RAM memory 808 (memory array), and RAM memory (memory array) associated with microprocessor 806, all connected together with buses so that the circuits are operational to share data therebetween. Ex. 1003, Fig. 13, 12:29–39.[24]

We adopt and incorporate Petitioner's showing as to claims 25–29, as set forth by the Petition and summarized above, as our own. *See* Pet. 7–20; 47–51. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 25–29 would have been obvious.

9. *Summary*

After a full review of the record, including Patent Owner's Response and Sur-reply and evidence, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, and Akasaka would have rendered obvious claims 1–30, 33, 36, and 38.

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[24] As discussed below (§ II.E.1), Trimberger provides another example of the prior art showing the direct connection between a large memory plane (block memory with 100,000 bits) and an FPGA for parallel reconfiguration in one cycle. Ex. 1006, 22–23, Fig. 1.

E. *Obviousness, Claims 31, 32, and 34*

1. *Trimberger*

Trimberger, titled "A Time-Multiplexed FPGA" (1997), describes an FPGA with on-chip memory distributed around the chip. Ex. 1006, 22. Trimberger teaches that the memory "can also be read and written by on- chip [FPGA] logic, giving applications access to a single large block of RAM." *Id.* Trimberger teaches this "storage [can] be used as a block memory efficiently." *Id.* at 28.

Trimberger's Figure 1 follows:

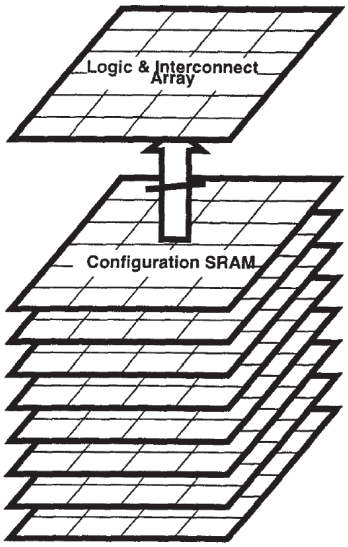

Figure 1. Time-Multiplexed FPGA Configuration Model

Figure 1 of Trimberger above depicts eight planes of SRAM (static random access memory) for an FPGA. *See* Ex. 1006, 22–23. "The configuration memory is distributed throughout the die . . . . This distributed memory can be viewed as eight *configuration memory*

planes (figure 1). Each plane is a very large word of memory (100,000 bits in a 20x20 device)." *Id.* at 22.

Trimberger also teaches accessing each plane of memory as one simultaneous parallel transfer of 100,000 memory data bits to reconfigure the FPGA quickly: "When the device is *flash reconfigured* all bits in logic and interconnect array are updated simultaneously from one memory plane. This process takes about 5ns. After flash reconfiguration, about 24ns is required for signals in the design to settle." Ex. 1006, 22.

2. *Claims 31, 32, and 34*

Petitioner contends claims 31, 32, and 34 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. *See* Pet 55–60. Except for the final limitations in independent claims 31 and 34, claims 31 and 34 recite limitations similar to claims 23 and 33. Petitioner relies on its showing with respect to claims 23 and 33 (addressed *supra* § II.D.6) to address the overlapping limitations of claims 31, 32, and 34. *See id.*

Claim 32 is materially similar to claims 24 and 30, as they each recite the same "functional to accelerate reconfiguration" clause. To address claim 32, Petitioner refers to and relies on its analysis of claim 24 (which relies on the analysis of claim 23). Pet. 47, 59. As indicated above in the analysis of claims 23, 24, 30, and 33, Patent Owner groups claim 32 with claims 24 and 30. *Supra* § II.D.6–7. For the reasons outlined above, Patent Owner's arguments with respect to claims 24 and 30 are unavailing. *Supra* § II.D.6–7. The same arguments with respect to claim 32 also are unavailing. *See id.*

Turning back to claims 31 and 34, limitation [31.4] and limitation [34.5] each recite "wherein said memory array is functional as block memory for said processing element." Petitioner relies on Trimberger's block memory teachings to address this limitation. *See* Pet. 58–60. According to Petitioner,

> Trimberger teaches that its co-located "memory is **accessible as block RAM** for applications," that are running in the FPGA, i.e., that the memory "can also be read and written by on-chip [FPGA] logic, giving applications access to a single large block of RAM." Ex. 1006, 22. Trimberger teaches that "the configuration storage to be used **as a block memory efficiently**." [*Id.* at 28].

Pet. 58 (emphasis by Petitioner) (quoting Ex. 1006, 22, 28). Petitioner contends that it would have been obvious to employ Trimberger's block memory to support fast local memory in FPGA applications like that in the combined teachings of Zavracky, Chiricescu, and Akasaka. *See id.* at 56–57 (citing Ex. 1002 ¶ 247; Ex. 1048). Petitioner also contends that "[t]he POSITA would have known that FPGAs have limited programmable logic space, and that for certain tasks it would be more cost-efficient and silicon-efficient to use the FPGA for reconfigurable processing and to use a separate task-dedicated memory element for block memory." *Id.* at 57 (citing Ex. 1002 ¶ 247). Petitioner advances other reasons for the combination. *See id.* at 57–58 (characterizing Trimberger's on-chip block memory as faster relative to off-chip memory).

Patent Owner argues that "[i]ndependent claims 31 and 34 . . . require that the 'memory array [that] is

functional as block memory' is on a separate chip from the 'first integrated circuit die element including a field programmable gate array.'" PO Resp. 44. According to Patent Owner "*Trimberger* . . . teaches away from having its block memory and FPGA on different chips as it attributes its quick FPGA reconfiguration to the massive connectivity ***within*** the chip." *Id.* (citing Ex. 1006, 22; Ex. 2011 ¶ 88); *see also id.* at 50 (same argument (citing Ex. 2011 ¶ 97)). Patent Owner primarily relies on this "within the chip" or "on-chip memory" argument as the basis for its allegations of lack of motivation, lack of a reasonable expectation of success, teaching away, requirement for major modifications, and other related arguments. *See id.* at 43–51.

For example, Patent Owner argues that "implementing Trimberger's FPGA structure in Petitioner's combination would result in a complete redesign of the hypothetical 3-D stacked structure of the *Zavracky- Chiricescu-Akasaka* Combination," because "the block memory is no longer stacked with the FPGA, but instead located on *Trimberger's* FPGA die as on-chip memory." Pet. 49 (citing Ex. 2011 ¶ 95). Patent Owner explains that "*Trimberger's* FPGA structure requires that its configuration memory planes are located on the same die as the FPGA's logic cells, so that the FPGA can quickly switch between different configurations." *Id.* at 50 (citing Ex. 2011 ¶ 97). Patent Owner asserts that "Petitioner admits this." *Id.* (characterizing the Petition as stating that Trimberger teaches a time multiplexed FPGA with on-chip memory distributed around the chip) (citing Pet. 56)). Based on these assertions, Patent Owner contends that evidence lacks as to "how or why a

POSITA would have had a reasonable expectation of success in making the combination." *Id.* at 45.

Petitioner persuasively shows that Trimberger does not teach away or support Patent Owner's related arguments based on the single-chip theory, including hypothetical re-designs, and lack of a reasonable expectation of success and motivation. Petitioner does not admit that Trimberger "requires that its configuration memory planes are located on the same die as the FPGA's logic cells." *See* PO Resp. 50 (citing Pet. 56); Pet. 56 (describing Trimberger's on-chip memory without characterizing it as a requirement).

Petitioner persuasively responds that Trimberger does not "criticize, discredit, or otherwise discourage investigation into the invention claimed," merely because it discloses embodiments having block memory and an FPGA within the same chip. Reply 22 (quoting *Depuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009)). Petitioner persuasively argues that Patent Owner's "'massive connectivity' observations about Trimberger confirm that the POSITA would have been further encouraged to make the combination." *Id.* at 23 (citing Ex. 1070 ¶¶ 44–45); *see* PO Resp. 50 (arguing Trimberger's block memory includes "massive connectivity" with the FPGA).

Petitioner's response, supported by Dr. Franzon's testimony, is persuasive. Trimberger's Figure 1 shows eight different memory planes on a single chip. Ex. 1006, 22. Trimberger states that "[t]he entire configuration of the FPGA can be loaded from this on-chip memory in 30ns." *Id.* Trimberger does not teach, and Dr. Souri does not testify, that Trimberger's "on-

chip memory" *requires* each memory plane to be on *the same layer* as the FPGA of a chip, such as a multi-layered chip or stack of chips. *See id.*; Ex. 2011 ¶ 97 (describing Trimberger as employing "massive connectivity ***within*** the chip").

Dr. Franzon explains credibly that "Trimberger's one-cycle teachings would be **improved** by applying its teaching to a 3D chip." Ex. 1070 ¶ 44. Dr. Franzon explains that Trimberger's reconfiguration clock cycle "(i.e., the delay in Trimberger) is set [by] determin[ing] the length of the longest path after routing." *Id.* (quoting Ex. 1006, 27). Then, Dr. Franzon testifies that "[t]he point here is that a shorter vertical interconnect allows for a shorter 'longest path' and a faster chip" and "[t]his was commonly understood in the other art." *Id.* (noting that "Akasaka taught that 3-D 'high speed performance' was enhanced because '[i]n 2-D ICs, the longest signal interconnection length becomes several to ten millimeters, but in 3-D ICs the length between upper and lower layers is on the order of 1–2 μm.'" (quoting Ex. 1005, 1705); also noting that Zavracky teaches that **"[i]n the proposed approach, shorter busses will result in smaller delays and higher speed circuit performance**" (quoting Ex. 1003, 3:4–14) (emphasis by Dr. Franzon)).

This testimony goes hand-in-hand with Petitioner's showing as summarized above in connection with claims 1, 17, and 23–25. That is, Petitioner shows persuasively that the combined teachings of Zavracky, Chiricescu, and Akasaka suggest short conductor runs using numerous distributed vias of a 3-D multi-layer chip to increase speed and bandwidth, decrease path delays, and

facilitate parallel processing. *See supra* §§ II.D.3–6, 8; Pet. 8–12 (background knowledge of an artisan of ordinary skill includes stacking chips with multiple distributed vias to minimize latency and maximize bandwidth), 16–20 (similar, listing multiple reasons to combine Zavracky, Chiricescu, Akasaka, including to accelerate data via shorter interconnection delay times, parallel processing, increased operating speed, etc.). The Petition also persuasively points to a "concern[] with the speed of access between the FPGA and the block of memory" as a reason to use Trimberger's "block memory . . . combined with Zavracky-Chiricescu- Akasaka's teaching of having the memory stacked and electrically coupled nearby." Pet. 57.

Supported by Dr. Franzon's testimony, Petitioner also persuasively responds that arranging a block memory on a separate layer from an (FPGA) processing element is not a major modification and the evidence shows that how to do it would have been well within the level of ordinary skill. *See* Reply 24; Ex. 1070 ¶ 46 ("Dr. Souri does not understand the combination being made. The Zavracky, Chiricescu, Akasaka combination already has a memory and an FPGA. It is already connected via a wide-area distributed set of interconnections as taught in Akasaka.").

Petitioner persuasively points to the Petition as stating that "[t]he POSITA would have sought Trimberger's teaching of using memory as a block memory and combined that with Zavracky-Chiricescu-Akasaka's teaching of having the memory stacked and electrically coupled nearby." Reply 24 (citing Pet. 57). In other words, Petitioner does not

propose "'***moving*** *Trimberger's* on chip memory" to the same layer as the FPGA in Zavracky-Chiricescu-Akasaka's stack, contrary to Patent Owner's argument. *See* PO Resp. 50; *see also* Sur-reply 20. Rather, Petitioner proposes modifying the existing memory of Zavracky's modified 3-D stack to function as a block memory according to Trimberger's teachings. *See* Pet. 57; Reply 24. Moreover, Trimberger's eight plane memory design suggests different layers at least for each plane of memory, and challenged claim 31 does not require more than one of Trimberger's block memory planes. *See* Pet. 54 (describing "us[ing] a separate task-dedicated memory element for block memory"); Ex. 1006, Fig. 1 (showing eight time multiplexed memory planes); Ex. 1070 ¶ 45 (testifying that in Trimberger's Figure 1 (*see supra* § II.E.1), "the fat arrow with a line in the traditional representation of 'many signals' – i.e., this is suggesting an architecture where different 'planes of memory' (i.e., layers of a die in a 3-D stack) are transferred from the configuration SRAMs to the FPGA").[25]

In any event, claims 31, 32, and 34 do not preclude eight separate memory layers in a stack, or all eight memory planes on the same layer in the stack, or a multiplexor to select the different memory

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[25] As summarized above, each memory plane in Trimberger contains 100,000 bits of memory. *Supra* § II.E.1. Also, "[w]hen the device is *flash reconfigured* all bits in logic and interconnect array are updated simultaneously *from one memory plane*. *Id.*; Ex. 1006, 22 (emphasis added). Contrary to Patent Owner's arguments in connection with claims 1 and 23– 25 discussed above, Trimberger provides another example of the prior art showing the connection of a large plane of memory (block memory) directly to an FPGA for reconfiguration in one cycle.

planes. Patent Owner essentially argues that an artisan of ordinary skill could and would have connected eight memory planes to an FPGA on a single layer as Trimberger describes to obtain a single reconfiguration of 100,000 bits, but such an artisan could and would not have connected the same circuits on separate layers together using vias with a reasonable expectation of success. The record shows otherwise, for the reasons outlined above.

Petitioner persuasively points to testimony by Dr. Franzon cited in the Petition, who in turn relies credibly on evidence of record, to show a reasonable expectation of success, showing that implementing block memory with an FPGA was well-known in the prior art. *See* Reply 24 (citing Pet. 57; Ex. 1002 ¶ 145, 248; Ex. 1003, Figs. 12, 13; Ex. 1003, 11:63–12:2; Ex. 1002 ¶ 145); Ex. 1002 ¶ 145 (testifying that "Cooke also discloses that the 'memory planes not being used for configuration may be used as memory,' i.e., an extra memory block for use by the FPGA" (citing Ex. 1032, 2:50–52), Ex. 1002 ¶ 144 (testifying that Casselman shows connecting "memory . . . directly to FPGA . . . through address and data busses." (citing Ex. 1026)).

As discussed above in connection with claims 1 and 23–25, Petitioner persuasively outlines several good reasons to combine related teachings from the references to arrive at a 3-D stack, reasons that apply to Trimberger's block memory. *See* Pet. 8–20, 55–58. For example, Petitioner notes that Trimberger teaches a block memory to provide access to a "single large block of RAM" such that memory "can . . . be read and written by on- chip [FPGA] logic." Pet. 58 (quoting Ex. 1006, 22). Petitioner also states that

implementing Trimberger's block memory teachings with the 3-D chip combination as suggested by Zavracky's "stack [of] memories together with processors or the programmable array" addresses "concern[s] with the speed of access between the FPGA and the block memory." *See id.* at 57. Petitioner notes that "FPGAs have limited programmable logic space" suggesting "a separate task-dedicated memory element for block memory." *Id.* Petitioner also persuasively argues that applying Trimberger as a separate layer of memory in the 3-D stack of Zavracky, Chiricescu, and Akasaka "would have merely been a combination of prior art elements according to known methods to yield a predictable result" and "would have been a well-known use of a memory," showing a reasonable expectation of success in "improv[ing] on the memory options of the FPGA." *Id.* As outlined above, the record supports Petitioner.

Patent Owner repeats or repackages its arguments addressed above, by arguing that "Trimberger does not cure any of the aforementioned deficiencies," "*Chiricescu* does not employ *Zavracky's* interconnections to connect a memory die to an FPGA die," and Petitioner does not show why or how "the modification would have been achieved with any reasonable expectation of success." *See* PO Resp. 46. Contrary to these arguments, as outlined above, Petitioner relies on the combined teachings of the references and the knowledge of an artisan of ordinary skill, and Trimberger provides more and persuasive evidence as to how and why an artisan of ordinary skill would have employed block memory as a single plane or several planes as separate layers in a 3-D stack, including to enhance reconfiguration speeds between a large block of memory and FPGA by

facilitating a large parallel data transfer of 100,000 bits in one clock cycle.

We adopt and incorporate Petitioner's showing as to claims 31, 32, and 34, as set forth by the Petition and summarized above, as our own. *See* Pet. 7–20, 55–60. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Trimberger would have rendered obvious claims 31, 32, and 34.

F. *Obviousness, Claims 35*

1. *Satoh*

Satoh, titled "Semiconductor Integrated Circuit, Method for Testing the Same, and Method for Manufacturing the Same," describes using an FPGA to generate test stimuli to test memory elements on the same chip. Ex. 1008, code (54). In one embodiment, Satoh describes

> a method for testing this semiconductor integrated circuit is such that, in a semiconductor integrated circuit incorporating a variable logic circuit (FPGA) for outputting a signal indicating whether or not a circuit is normal [wherein] . . . a memory test circuit is built for testing the memory circuits in accordance with a specified algorithm . . . without using an external high-performance tester.

Ex. 1008, 46.[26]

Satoh also describes a "memory array" and testing DRAMs (dynamic random access memory arrays) such that "a test circuit . . . for testing the DRAMs 150 to 180 is formed in the portion of the FPGA 120 . . . , and the DRAMs 150 to 180 are tested in succession." *See* Ex. 1008, 15, Fig. 7.

2. *Claim 35*

Petitioner contends claim 35 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Satoh. *See* Pet. 60–63. Claim 35 is similar to claims 23 and 33 (*see supra* § II.D.6), including an FGPA electrically coupled to a memory array stacked therewith by a number of distributed contact points, but unlike claims 23 and 33, claim 35 does not include the "functional to accelerate" "wherein" clause and instead includes the following "functional to provide test stimulus" "wherein" clause: "wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit die element."

Petitioner relies on its showing with respect to the "Zavracky- Chiricescu-Akasaka Combination," which includes its showing for claims 23 and 33. *See* Pet. 61 (citing Ex. 1002 ¶¶ 240–245), 62–63 (referring to its analysis of claim 33, which materially tracks its claim 23 analysis). According to Petitioner, "[i]t was well-known to test stacked modules in order to avoid the expense and waste of silicon by creating 'dead' chips, and improve yield." *Id.* (citing Ex. 1002 ¶¶ 240–

[26] Page citations refer to original page numbers.

245; Ex. 1009; Ex. 1043). Petitioner states that "Satoh specifically praised the use of an FPGA to test 'memory circuits' for 'improving yield and productivity of the semiconductor integrated circuit.'" *Id.* (quoting Ex. 1008, 47:23–27).

Addressing the "functional to provide test stimulus" "wherein" clause, Petitioner explains that Satoh describes an FPGA that "generates a specified test signal [and] supplies the test signal to the memory circuit." Pet. 63 (citing Ex. 1002 ¶¶ 350–359; Ex. 1008, 5:1–28, 49:32–37). Petitioner maintains that Satoh's test signal suggests a "test stimulus" to a second integrated circuit memory array to evoke a response therefrom. *See id.* (citing Ex. 1008, 49:32–37; Ex. 1002 ¶ 358). Based on Satoh's teaching, Petitioner explains that "[i]n the Zavracky-Chiricescu-Akasaka-Satoh Combination," it would have been obvious to implement "the test signal . . . through the contact points between the FPGA of the first IC die element and the memory of the second IC die element," because that "is how those elements are stacked and electrically coupled." *See id.* (citing Ex. 1002 ¶ 359).

In addition to avoiding "dead chips," Petitioner cites other reasons to combine Satoh's testing functionality with the 3-D chip of Zavracky-Chiricescu-Akasaka:

> Recognizing the need to test the 3D stack of the Zavracky- Chiricescu-Akasaka Combination, the POSITA would have sought out Satoh's teaching of using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity. Ex.

> 1002 ¶242. Moreover, (4) a FPGA is reusable: after being configured for testing in manufacture, the FPGA would then be reconfigured for its normal "in the field" purpose. *Id.* (citing Ex. 1045 ("Another advantage . . . is that after testing is complete, the reconfigurable logic (FPGA 28) can be reconfigured for post- testing adapter card functions."); Ex. 1046).

Pet. 61–62.

Petitioner also relies on the following evidence and rationale to support a reasonable expectation of success:

> It was well known to use a FPGA to test circuitry with 2-D chips as taught by Satoh. Ex. 1002 ¶241 (citing Ex. 1043). The POSITA would have recognized Satoh's teaching would readily apply to the 3-D chip elements in the Zavracky-Chiricescu- Akasaka Combination. This includes because such a combination would have been a routine use of an FPGA, whose testing ability was not dependent on structure. Ex. 1002 ¶¶242–43. The result of this combination would have been predictable, by known FPGA testing to the 3D stack according to known methods to yield a predictable result. Ex. 1002 ¶244.

Pet. 62.

Patent Owner relies on the same unavailing arguments it advances with respect to claims 1 and 23–25 that we address above. *See* PO Resp. 51 ("Because Petitioner does not contend that *Satoh* cures any of the deficiencies of the combination of *Zavracky*, *Chiricescu,* and *Akasaka,* as discussed

above with respect to Ground 1, its reliance on the same rationales for Ground 3 also fail.")

Patent Owner also argues that "Petitioner's contention that a POSITA would be motivated to make the combination because it was well-known to test stacked die and Satoh tested memory elements on the same semiconductor chip (*see* Petition at 60–61) is divorced from the claimed invention." PO Resp. 52. Patent Owner contends that "Petitioner's generic rationale for using FPGAs for testing is wanting in particularity as to why a POSITA would combine the references as recited in the Challenged Claim." *Id.* Patent Owner contends that "[w]hether the use of *Satoh's* FPGA is beneficial for testing does not sufficiently explain why a POSITA would have combined the references to yield the claimed invention." *Id.* at 53. Patent Owner contends that Petitioner's rationale fails "as it lacks sufficient motivation of how or why a POSITA would have been motivated to use Satoh's FPGA for testing with the hypothetical 3-D structure of *Zavracky- Chiricescu-Akasaka* 'in the way the claimed invention does.'" *Id.* (quoting *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012)).

Patent Owner's arguments appear to accept Petitioner's showing that applying Satoh's testing structure and technique in "the hypothetical 3-D structure of *Zavracky-Chiricescu-Akasaka*" would have been "beneficial" and "predictable." *See* PO Resp. 52–53. That is, Patent Owner characterizes the rationale as "generic" without disputing it. *See id.*

In any event, Petitioner provides specific reasons related to specific recitations in the claims as outlined above, including tying Satoh's testing of a memory

array using FPGA testing circuitry to the similar claim elements in claim 35. For example, using Satoh's FPGA test circuitry and memory testing teachings to avoid "dead chips" is a specific "beneficial" reason, and tying these teachings to FPGA contact points in the Zavracky-Chiricescu-Akasaka" stack to test memory in that stack also is specific. *See* Reply 25 (re-listing reasons supplied in the Petition, including, for example, "the known problem of the need to test stacked modules to avoid the expense and waste of silicon by creating 'dead' chips" (citing Ex. 1002 ¶ 241; Ex. 1009; Ex. 1020; Ex. 1043); Pet. 63 (explaining that "[i]n the Zavracky-Chiricescu- Akasaka-Satoh Combination, the test signal is sent through the contact points between the FPGA of the first IC die element and the memory of the second IC die element, which is how those elements are stacked and electrically coupled" (citing Ex. 1002 ¶ 359)). As Dr. Franzon also credibly explains, Satoh's use of generating a test signal "*within* an FPGA" to test a memory array is agnostic "to the particular way in which the FPGA is stacked." *See* Ex. 1002 ¶ 245 ("The POSITA would thus have realized that Satoh could be used to solve the existing need (which was also recognized by Ex.1043, for example) to achieve the benefits discussed above.").

In other words, Petitioner persuasively shows a reasonable expectation of success with specific reasons to combine, all supported by the record, including beneficial testing to avoid dead chips and maintain reliable memory to reconfigure the 3-D stack's FPGA post-manufacture, thereby showing how to apply the teachings to the claimed 3-D stack as suggested by Zavracky, Chiricescu, and Akasaka. Specifically, claim 35 recites "wherein said contact

points are further functional to provide test stimulus from said [FPGA] to said at least second integrated circuit die element," and Petitioner persuasively applies Satoh's teachings to these contact points in order to avoid dead chips. Another set of specific and persuasive reasons to combine is "using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity." Pet. 61.

As Petitioner also persuasively argues, Petitioner's "evidence-backed assertions are uncontroverted, specific to relevant teachings of the references, and explain why a POSITA would have sought the Zavracky- Chiricescu-Akasaka-Satoh Combination to reach the '035 patent's claims." Reply 25 (citing Ex. 1070 ¶¶ 76–77).

Patent Owner advances a new (unresponsive) argument in its Sur- reply that "[t]he references Petitioner and Dr. Franzon cite do not disclose testing of 3-D stacked processor but instead disclose that individual die are tested independently and prior to any 3D packaging." Sur-reply 22. This argument is not relevant to a claim limitation at issue here. Claim 35 does not require packaging or preclude "provid[ing] test stimulus from said field programmable gate array to said at least second integrated circuit die element" prior to any packaging.

We adopt and incorporate Petitioner's showing as to claim 35, as set forth by the Petition and summarized above, as our own. *See* Pet. 7–20, 60–63. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that tend to

overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Satoh would have rendered obvious claim 35.

G. *Obviousness, Claim 37*

1. *Alexander*

Alexander, titled "Three-Dimensional Field-Programmable Gate Arrays" (1995), describes "stacking together a number of 2D FPGA bare dies" to form a 3-D FPGA. Ex. 1009, 253. Alexander explains that "each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die." *Id.*

Alexander's Figure 2 follows:

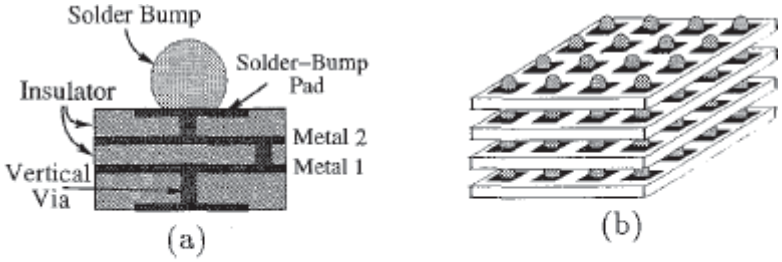

Figure 2: (a) The solder bump, pad, and vertical via geometry; and (b) stacked 2D FPGA dies.

Figure 2(a) shows vertical vias traversing a chip with a solder pad and solder bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1009, 253.

Alexander explains that stacking dies to form a 3-D FPGA results in a chip with a "significantly

smaller physical space," lower "power consumption," and greater "resource utilization" and "versatility" as compared to conventional layouts. Ex. 1009, 253.

2. *Claim 37*

Claim 37 depends from independent claim 36 and recites "[t]he programmable array module of claim 36 wherein said third integrated circuit die element includes another field programmable gate array." As noted above, independent claim 36 is similar to independent claims 1, 17, and 23, and Petitioner refers to its showing of claims 1, 5, and 23 to address claim 36. *See supra* §§ II.D.4, 6; Pet. 53. Through its dependency from claim 36, claim 37 essentially recites three stacked integrated circuit die elements, the first one "including" an FPGA, the second one "including" a memory array, with "said first and second integrated circuit die elements being coupled by a number of contact points distributed throughout the surfaces of said die elements," and "a third integrated circuit die element includ[ing]" "another" FPGA "stacked with and electrically coupled to at least one of said first or second integrated die elements." Therefore, the module of claim 37 essentially requires two FPGAs and a memory array, with the circuit that includes one of the FPGAs simply "electrically coupled" to one of the circuits that includes the other FPGA or memory array, and the latter circuits "coupled by a number of contact points distributed throughout the surfaces of said die elements."

Petitioner contends claim 37 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Alexander. *See* Pet. 63–66. Addressing the two stacked FPGAs of claim 37, Petitioner relies

on Alexander's teaching of stacked FPGAs in a 3-D package, and contends as follows:

> The POSITA would have known (as Zavracky notes) that multiprocessor systems were needed for "parallel processing applications," for example, "signal processing applications." Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶258. But in this context, the POSTIA would have appreciated Alexander's teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). The POSITA would have sought out Alexander's multiple stacked FPGAs to enhance the Zavracky-Chiricescu-Akasaka Combination by upgrading it for this type of application. 1002 ¶259.

Pet. 65.

Petitioner contends that Alexander's similar structure of multiple stacked FPGAs, as similar to multiple processors stacked with multiple memories of the Zavracky-Chiricescu-Akasaka Combination, evidences a reasonable expectation of success of stacking FPGAs with memories, with multiple dies stacked and vertically interconnected including using thousands of contact point vias (holes)." *See* Pet. 65. Petitioner also asserts that "[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to known methods to yield a predictable result." *Id.* (citing Ex. 1002 ¶¶ 260–261).

Patent Owner responds that "[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no bearing on whether a POSITA would have been motivated to combine *Alexander* with *Zavracky-Chiricescu-Akasaka* to reach a 3-D processor module having 'a third integrated circuit die element [that] includes another field programmable gate array.'" PO Resp. 54–55 (citing Ex. 2011 ¶ 100). This argument appears to accept Petitioner's showing that FPGAs are preferable to processors in a 3-D stack. Petitioner's unchallenged showing of faster FPGAs relative to general purpose processors in the 3-D stack of Zavracky-Chiricescu-Akasaka, where Zavracky contemplates multiple layers of processors, memory layers, and an FPGA, is a persuasive reason for the combination. *See* Ex. 1003, Fig. 12 (stacked multiple processor and memory layers/chips), Fig. 13 (stacked processor, memory, and PLA/FPGA layers/chips).

Patent Owner also argues that Petitioner's "conclusory rationale is further discredited by Petitioner's suggestions elsewhere in the Petition that *Chiricescu* discloses a FPGA application that enhances *Zavracky*." PO Resp. 55. In particular, Patent Owner argues that the Petition elsewhere suggest that a "POSITA would have taken Chiricescu's suggestion of a FPGA to perform 'arbitrary logic functions,' . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in Zavracky, e.g., to perform image and signal processing tasks that would have taken advantage of co-stacked microprocessors and memories as taught in Zavracky." *Id.* (quoting Pet. 18). Patent Owner argues that "there is no reason . . . to combine *Alexander* with *Zavracky- Chiricescu-*

Akasaka," because "Petitioner acknowledges that, *Chiricescu*, like *Alexander*, offers FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor." *Id.* (citing Ex. 2011 ¶ 101).

Patent Owner's arguments are unavailing. For example, Patent Owner concedes that "*Chiricescu*, like *Alexander*, offers FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor." PO Resp. 55. Dependent claim 37 does not preclude employing a microprocessor, because it is open-ended and recites "comprising" and "at least" a "first," "second," and "third integrated circuit functional element." To address claim 37, Petitioner specifically and persuasively argues that "[t]he POSITA would have known (as Zavracky notes) that *multiprocessor* systems were needed for 'parallel processing applications,' for example, 'signal processing applications.'" Pet. 65 (citing Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶ 258). Petitioner also repeatedly points to Zavracky's microprocessors 804 and 806 in Figure 13 to address claim 1, reproduces Figure 13 in addressing claim 23 (which it relies upon to address independent claim 36), and refers to the "Zavracky-Chiricescu-Akasaka Combination." *See id.* at 44–45 (quoting Zavracky as stating that its "invention relates to the structure [of] vertically stacked and interconnected circuit elements for . . . programmable computing." (citing Ex. 1003, 12:28–38, Fig. 13), 53 (referring to its analysis of claims 1, 5, and 23 to address claim 36). Therefore, Patent Owner's characterization that Chiricescu and Alexander "offer[] FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor" and Petitioner's argument that

Chiricescu suggests FPGAs for performing arbitrary logic functions and expanding packet processing tasks with microprocessors, are specific and persuasive reasons to employ FPGAs in the stack of Zavracky-Chiricescu- Akasaka-Alexander. *See* PO Resp. 55; Pet. 18.

In other words, as Petitioner also persuasively argues, "[a]s to the 'why,' the Petition shows that (i) the POSITA would have been prompted to pursue a 'multiprocessor system' to facilitate 'parallel processing applications'; and (ii) the POSITA would have viewed Alexander's "stacked FPGAs as preferable over alternatives" for achieving such a system." Reply 26 (citing Pet. 65; Ex. 1002 ¶¶ 257–61). "And as to the 'how,' the Petition explains that 'the POSITA would have realized that using multiple FPGA dies in the stack as taught by Alexander would work in a straightforward manner similar manner to stacking multiple memories, or multiple microprocessors, as already taught in the Zavracky-Chiricescu-Akasaka Combination.'" *Id.* (quoting Pet. 65).

Patent Owner also alleges that the Petition fails to explain how to combine the references with a reasonable expectation of success. PO Resp. 55–57. Patent Owner alleges that other sections of *Alexander* . . . [that] Petitioner wholly ignores . . . . do not suggest . . . that using multiple FPGA dies would work in a straightforward manner, let alone in Petitioner's proposed combination, so as to have a reasonable expectation of success." *Id.* Patent Owner provides little support for this argument. *See id.* Contradicting Patent Owner, Alexander itself states that using multiple FPGAs in a stack results in a chip

with "significantly smaller physical space," lower "power consumption," "shorter signal propagation delay," and "greater resource utilization and versatility" due to the "increased number of logic block neighbors" as "compared with a circuit-board-based 2D FPGA implementation." Ex. 1009, 253. In other words, Alexander suggests that stacked FPGAs simply implement the same circuitry of well-known single layer FPGAs, albeit with numerous advantages.

Patent Owner also refers to sections in Alexander that describe thermal issues. PO Resp. 56. Patent Owner also argues that "Petitioner's threadbare argument that the combination is based on known methods to yield a predictable result (*see* Petition at 65) is . . . untethered to the features of the claimed invention." *Id.* at 57.

Contrary to these arguments, the Petition tethers the claimed stacking of two FPGAs to several reasons to combine the references. As discussed above, Patent Owner itself cites these reasons offered by Petitioner, including "offer[ing] FPGAs to enhance parallel processing image and signal tasks of *Zavracky's* microprocessor," and similarly "perform[ing] 'arbitrary logic functions,' . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in *Zavracky*," as noted above. *See* PO Resp. 55 (citing Pet. 19).

As Petitioner also argues, Patent Owner does not dispute that "Zavracky already taught combining an FPGA with a memory and microprocessor." Reply 27 (citing Ex. 1003, 12:29–39, Fig. 13). Adding another FPGA layer in place of one of the microprocessor layers in Zavracky (Ex. 1003, Figs. 12, 13) therefore

would have reduced thermal problems, "because FPGAs were more energy-efficient than microprocessors for the same size die, reducing heat." *Id.* at 28 (citing Ex. 1070 ¶¶ 37–41; Ex. 1058; Ex. 1082). Dr. Franzon's testimony includes an excerpt from DeHon (Ex. 1058) and Scrofano (Ex. 1082), which support Dr. Franzon's testimony that "FPGAs needed less power to get the same level of computing capability" as a processor. *See* Ex. 1070 ¶¶ 37–38 (citing Ex. 1058, 43). Similar to Alexander's teaching that "3D FPGAs have good implications with respect to power consumption" (Ex. 1009, 263), the '035 patent also evidences that 3-D stacks "overall reduced power requirements" (Ex. 1001, 4:63). Reduced power translates to less heat, as was well-known and as Petitioner shows. *See infra* note 27.

Describing dual layer FPGA stacks, the '035 patent states as follows:

> It should be noted that although a single FPGA die 68 has been illustrated, *two or more FPGA die 68 may be included in the reconfigurable module 60. Through the use of the through- die area array contacts 70*, inter-cell connections *currently limited to two dimensions of a single die*, may be routed up and down the stack in three dimensions. *This is not known to be possible with any other currently available stacking techniques since they all require the stacking contacts to be located on the periphery of the die.* In this fashion, the number of FPGA die 68 cells that may be accessed within a specified time period is increased by up to 4 VT/3, where "V" is the propagation velocity of the wafer and "T" is the specified time of propagation.

Ex. 1001, 5:11–24 (emphasis added). Here, the '035 patent offers no description of any specific connection scheme between the two FPGA dies. It simply describes vias throughout the periphery of each die (instead of just at the periphery thereof) as a new technique (which is not correct), without any mention of heat problems associated with stacking two FPGAs. The '035 patent's lack of description and focus on vias throughout the whole die as a solution (providing speed gains) further evidences a reasonable expectation of success and supports Petitioner's showing.

As Petitioner also argues, thermal issues were a routine consideration, with known viable options to address the issues. Reply 28 (citing Ex. 1020, 11; Ex. 1070 ¶¶ 29–41; Ex. 1020; Ex. 1012; Ex. 1009; Ex. 1058; Ex. 1082). Dr. Franzon credibly lists known ways to dissipate heat, including use of low thermal resistance substrates, forced fluid coolants, thermal vias, and thermally conductive adhesives. Ex. 1070 ¶ 32.

The record also supports Dr. Franzon's testimony that "Alexander itself noted that thermal concerns were standard in any multi-chip design."[27] In addition to mitigating heat concerns by eliminating I/O buffers (or "restrict[ing] I/O to one layer and plac[ing] it close to the heat sink," Ex. 1009, 256 § 5), in the same section, Alexander further supports Dr. Franzon's

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[27] Testimony from footnote 2 of Dr. Franzon's declaration follows: "It would have been well known to the POSITA that in a chip, an increase in power usage generally translated to an increase in heat. For example, a processor using more power to perform computations will put off more heat than when the processor is using less power."

testimony, stating that "[a] number of . . . thermal-reduction techniques (i.e., thermal bumps and pillars . . ., thermal gels . . ., etc.) may also be applicable for 3D FPGAs." Ex. 1009, 255 § 5 ("Thermal Issues"). Alexander also states that "[a]s the power-to-area/volume ratio increases, so does the operating temperature unless heat can be effectively dissipated." *Id.*

As Petitioner also persuasively reasons, Patent Owner's arguments about heat dissipation concerns here do not undermine Petitioner's showing of a reasonable expectation of success, because a reasonable expectation of success "does not require a certainty of success." Reply 28 (quoting *Medichem v. Rolabo S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006)). As found above, Alexander promotes using multiple FPGAs in a module stack, and myriad additional evidence further supports a reasonable expectation of success. *See id.* (citing Ex. 1002 ¶¶ 44–45 (listing prior art showing FPGA stacks or FPGA stacks with microprocessors and memory), ¶¶ 260–261; Ex. 1009, 1).

Finally, none of the challenged claims, including claim 37, specifies the size of the claimed 3-D modules or corresponding amount of computing power. Therefore, the breadth of claim 37 encompasses a 3-D stack operable on a minimal power basis (and without any limit on the area of each die, further dissipating heat as the chip area increases), rendering heat concerns nonexistent or at least well within the bounds of a reasonable expectation of success. *See supra* note 27; Ex. 1009, 255–256 § 5 (discussed above, e.g., as power per unit area decreases, so does temperature).

We adopt and incorporate Petitioner's showing as to claim 37, as set forth by the Petition and summarized above, as our own. *See* Pet. 7–20; 63–66. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Alexander would have rendered obvious claim 37.

H. *Exhibit 1070*

Patent Owner argues that "[p]aragraphs 5–9, 13–28, 29–41, 44, 45, 59–66, 68, 73, 74, 76, 77, and 94–103 from Dr. Franzon's [Reply D]eclaration (Ex. 1070) addressing Petitioner's alleged obviousness grounds are not sufficiently discussed in the Reply" at pages 10, 14, 20, 21, 25, 27, and 28 of the Reply. Sur-reply 25. Patent Owner contends that the noted paragraphs are "not discussed in the Reply, but instead incorporated by citation or a cursorily parenthetical." *Id.* Patent Owner further contends that "the Board should not and cannot play archeologist with the record to search for the arguments" and "should not . . . consider[] Dr. Franzon's arguments." *Id.* (citing 37 C.F.R. § 42.6(a)(3) ("Arguments must not be incorporated by reference from one document into another document.").

Patent Owner also cites *General Access Solutions, Ltd. v. Sprint Spectrum L.P.*, 811 F. App'x 654, 658 (Fed. Cir. 2020) as "upholding the Board's finding of improper incorporation by reference because, *inter alia*" (Sur-reply 25), "'playing archaeologist with the record' is precisely what the rule against

incorporation by references was intended to prevent," (*id.* (quoting *Spring Spectrum*, 811 F. App'x at 658, internal citation omitted)). The situation here is different than in *Sprint Spectrum*, because there, the court noted a problem with identifying a party's substantive arguments *prior to turning to the declaration at issue*: "*To identify GAS's substantive arguments*, the Board was forced to turn to a declaration by Struhsaker, *and further to delve into a twenty-nine-page claim chart attached as an exhibit*." *Id.* (emphasis added).

Here, Patent Owner does not describe or allege any problem with identifying Petitioner's substantive arguments. In context, except as discussed below, the cited paragraphs of Dr. Franzon's Reply Declaration (Ex. 1070) properly support Petitioner's substantive arguments at the pages of the Reply identified by Patent Owner.

Regarding the first citation, page 10 of the Reply cites paragraphs 94– 103 of Dr. Franzon's Reply Declaration, and discusses how, even if the "functional to accelerate" clauses require "a wide configuration data port," the combination of Zavracky, Chiricescu, and Akasaka teaches it. *See* Reply 9–10 (citing Ex. 1070 ¶¶ 94–103). This citation is a misprint or oversight by Petitioner, because Dr. Franzon's Reply Declaration does not include paragraphs 96–102. Therefore, any issue with respect to those paragraphs is moot. The remaining cited paragraphs of Dr. Franzon's Reply Declaration on page 10 of the Reply directly relate to what a "wide configuration data port" constitutes. Also, paragraph 95 reproduces some of the same testimony by Dr. Chakrabarty (Patent Owner's expert in IPR2020-

01021) that the Reply discusses and reproduces on page 10 of the Reply.

Regarding the second citation, page 14 of the Reply cites two paragraphs with a parenthetical as follows: "Ex. 1070 ¶¶ 73–74 (citing Ex. 1083, an example of common usage of 'share data' as 'transfer data')." Prior to the citation, the Reply addresses the plain meaning of "share," tracking the parenthetical. *See* Reply 14. Notwithstanding that Patent Owner generally implies that citation is one of several examples of "a cursorily parenthetical" (Sur-reply 25), the parenthetical is clear as to how Dr. Franzon's cited testimony supports Petitioner's Reply argument.

Regarding the third citation, page 20 of the Reply (citing Ex. 1070 ¶¶ 13–28), Petitioner's argument merely responds to a summary argument by Patent Owner about four different "TSV interconnection issues." *See* PO Resp. 41 ("At the time of the invention, a POSITA was aware of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ('HDL') algorithms, which must be considered." (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89); Reply 20 ("The supposed 'TSV interconnection issues' that [Patent Owner] cursorily identifies were at most normal engineering issues, not problems preventing a combination. Ex. 1070 ¶¶ 13–28 (Dr. Franzon rebutting Dr. Souri's testimony as to every purported issue with citations to evidence)." Here, Petitioner's parenthetical generally informs the reader that Dr. Franzon's testimony responds to Dr. Souri's "cursor[y]" summary alleging "TSV interconnection issues." *See* Reply 20; PO Resp. 41.

Paragraphs 13–20 of Dr. Franzon's Reply Declaration provide background context leading to thrust of paragraphs 21–28, which directly support Petitioner's Reply argument that TSV issues were normal engineering issues in the context of combining the references. Therefore, we consider cited paragraphs 13–20 only as background information and context.

In comparison, providing his testimony about the TSV issues, Dr. Souri's support for TSV issues is a citation to "Ex. 2014 at 85, 97, 90." Ex. 2011 ¶ 82. Patent Owner provides the same citation without any explanation of the citation. PO Resp. 41. This amounts to the same type of incorporation-by-reference of pages of evidence that Patent Owner attributes to Petitioner. Also, the cited three pages of Exhibit 2014 are in the middle of an industry article, and the pages are densely packed two-column pages that facially appear to have at least the same number of words in some of the complained-about citations to multiple paragraphs that Petitioner provides to Dr. Souri's Reply Declaration. Here, Patent Owner leaves it to the Board to dig into the cited pages of Exhibit 2014 to find the alleged TSV interconnection issues and place it in context to the background information in the whole article. In reaching our decision, we exercised judgment as to all the evidence cited by the parties for its relevance, context, and substance, and weighed it accordingly.

Finally, an examination of the other citations identified by Patent Owner in full context, reveals (like the citations addressed above) that Petitioner's use of and citation to Dr. Souri's testimony is not improper. In summary, the remaining pages of the

Reply identified by Patent Owner include citations with a clear sentence preceding the citation and/or clear parenthetical informing the reader clearly how the cited testimony supports the sentence. *See* Reply 21 n.7 (clear parenthetical and preceding sentence (citing Ex. 1070 ¶¶ 59–66)), 25 (clear preceding sentence (citing Ex. 1070 ¶¶ 76–77), 27 (no citation), 28 (clear parentheticals and preceding sentences about thermal issues (citing Ex. 1070 ¶¶ 37–41; Ex. 1070 ¶¶ 29–41)).[28]

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.[29] In summary:

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[28] As noted above, Patent Owner cites to page 27 of the Reply, but page 27 does not have a citation to Exhibit 1070. It appears that Patent Owner intended to refer to the two citations to Exhibit 1070 on page 28 of the Reply. *See* PO Resp. 25; Reply 28.

[29] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent -able
1–30, 33, 36, 38	103(a)	Zavracky, Chiricescu, Akasaka	1–30, 33, 36, 38	
31, 32, 34	103(a)	Zavracky, Chiricescu, Akasaka, Trimberger	31, 32, 34	

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent -able
35	103(a)	Zavracky, Chiricescu, Akasaka, Satoh	35	
37	103(a)	Zavracky, Chiricescu, Akasaka, Alexander	37	
Overall Outcome			1–38	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–38 the '035 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2

APPENDIX G

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

IPR2020-01571[1]
Patent 6,781,226 B2

XILINX, INC., and TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD., PETITIONER,

v.

ARBOR GLOBAL STRATEGIES, LLC, PATENT OWNER

Entered: Mar. 2, 2022

FINAL WRITTEN DECISION

35 U.S.C. § 318(a)

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

FENICK, *Administrative Patent Judge*.

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[1] Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00738 and has been joined as a party to IPR2020-01571. *See also* Paper 38 (order dismissing-in-part Taiwan Semiconductor Manufacturing Co. Ltd. as a party with respect to claims 13, 14, 16–23, and 25–30).

Xilinx, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–30 (the "challenged claims") of U.S. Patent No. 6,781,226 B2 (Ex. 1001, "the '226 patent"). Petitioner filed a declaration of Dr. Paul Franzon (Ex. 1002) with its Petition. Arbor Global Strategies LLC ("Patent Owner"), filed a Preliminary Response (Paper 7). We determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims and we instituted this proceeding on March 5, 2021, as to all challenged claims and all grounds of unpatentability. Paper 12 ("Dec. on Inst.").

After institution, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp.") and a declaration of Dr. Shukri J. Souri in support (Ex. 2006); Petitioner filed a Reply (Paper 22, "Pet. Reply") and a second declaration of Dr. Franzon in support (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 26, "PO Sur-reply"). Thereafter, the parties presented oral arguments, and the Board entered a transcript into the record. Paper 32 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(b)(4). For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies only itself. Pet. 69. Taiwan Semiconductor Manufacturing Co. Ltd. identifies itself and TSMC

North America as real parties-in-interest. *See* IPR2021-00393, Paper 1, 69. Patent Owner identifies only itself as a real party-in-interest. Paper 4, 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC v. Xilinx, Inc.*, No. 19-CV-1986-MN (D. Del.) (filed Oct. 18, 2019) as a related infringement action involving the '226 and three related patents, U.S. Patent No. RE42,035 E (the "'035 patent"), U.S. Patent No. 7,282,951 B2 (the "'951 patent") and U.S. Patent No. 7,126,214 B2 (the "'214 patent"). *See* Pet. 69; Paper 4, 1. Petitioner "contemporaneously fil[ed] [*inter partes* review] petitions challenging claims in each of these patents," namely IPR2020- 01567 (challenging the '214 patent), IPR2020-01568 (challenging the '951 patent), and IPR2020-01570 (challenging the '035 patent). Pet. 69.

The parties also identify *Arbor Global Strategies LLC* v. *Samsung Electronics Co., Ltd.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) ("the Samsung action") as a related infringement action involving the '035, '951, and '226 patents. Pet. 69; Paper 4, 1. Subsequent to the complaint in the Samsung action, Samsung Electronics Co., Ltd. ("Samsung") filed petitions challenging the three patents, and the Board instituted on all challenged claims, in IPR2020-01020, IPR2020-01021, and IPR2020-01022 ("the 1022IPR"). *See* IPR2020-01020, Paper 11 (decision instituting on claims 1, 3, 5–9, 11, 13–17, 19– 22, 25, 26, 28, and 29 of the '035 patent)); IPR2020-01020, Paper 30 (final written decision finding all challenged claims unpatentable); IPR2020-01021, Paper 11 (decision instituting on challenged claims 1, 4, 5, 8, 10, and 13–15 the '951 patent);

IPR2020-01021, Paper 30 (final written decision finding all challenged claims unpatentable); IPR2020-01022, Paper 12 (decision instituting on challenged claims 13, 14, 16–23, and 25–30 of the '226 patent) (Ex. 2004); IPR2020-01022, Paper 34 (final written decision finding all challenged claims unpatentable).

C. *The '226 Patent*

The '226 patent describes a stack of integrated circuit (IC) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '226 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." *Id.*

Figure 4 follows:

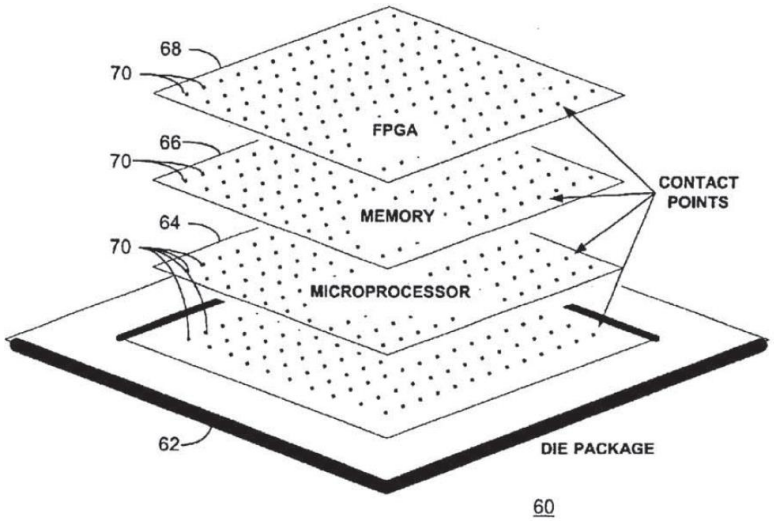

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64, interconnected using contact holes 70. *Id.* at 4:9–33.

The '226 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:19–35. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA), making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See id.* A "reconfigurable processor" provides a known benefit of flexibly providing the specific functional units needed for applications to be executed. *See id.*

D. *Illustrative Claims 1 and 10*

The Petition challenges claims 1–30. Of these claims, 1, 7, 13, and 22 are independent and claims 2–

6, 8–12, 14–21, and 23–30 depend from one of the challenged independent claims either directly or indirectly. Claims 1, 7, 13 and 22, reproduced below with bracketed numbering added for reference, illustrate the challenged claims at issue:

> 1. A processor module comprising:
>
> [1.1] at least one field programmable gate array integrated circuit die element including a programmable array; and
>
> [1.2] at least one microprocessor integrated circuit die element stacked with and electrically coupled to said programmable array of said at least one field programmable gate array integrated circuit die element,
>
> [1.3] such that processing of data shared between the microprocessor and the field programmable gate array is accelerated.

Ex. 1001, 6:16–26.

> 7. A processor module comprising:
>
> at least one field programmable gate array integrated circuit die element including a programmable array; and
>
> at least one microprocessor integrated circuit die element stacked with and electrically coupled to said programmable array of said at least one field programmable gate array integrated circuit die element,
>
> [7.3] the at least one field programmable gate array integrated circuit die element being configured to provide test stimulus to the

at least one microprocessor integrated circuit die element during manufacture and prior to completion of the module packaging.

Ex. 1001, 6:45–57, Cert. of Corr.

13. A processor module comprising:

at least a first integrated circuit die element including a programmable array;

at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[13.4] means for reconfiguring the programmable array within one clock cycle.

Ex. 1001, 7:9–22.

22. A processor module comprising:

at least a first integrated circuit die element including a programmable array and a plurality of configuration logic cells;

at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[22.4] means for updating the plurality of configuration logic cells within one clock cycle.

Ex. 1001, 8:4–17.

E. *The Asserted Grounds*

Petitioner challenges claims 1–30 of the '226 patent on the following grounds (Pet. 1):

Claims Challenged	35 U.S.C. §	References
1–6	103[2]	Zavracky,[3] Chiricescu,[4] Akasaka[5]
7–12	103	Zavracky, Chiricescu,

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Petitioner and Patent Owner each use December 5, 2001 in their analysis. Pet. 3, 5; Ex. 1002 ¶¶ 27–29; PO Resp. 10; Ex. 2006 ¶ 25. We assume that the '226 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment) and that the pre-AIA version of § 103 applies.

[3] Zavracky et al., US 5,656,548, issued Aug. 12, 1997. Ex. 1003.

[4] Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98. Ex. 1004.

[5] Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Iss. 12, pp. 1703–1714, Dec. 1986, ISSN 0018-9219. Ex. 1005.

Claims Challenged	35 U.S.C. §	References
		Akasaka, Satoh[6]
13–30	103	Zavracky, Chiricescu, Akasaka, Trimberger[7]

II. ANALYSIS

Petitioner challenges claims 1–30 as obvious based on the grounds listed above. Patent Owner disagrees.

A. *Legal Standards*

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

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[6] Satoh, PCT App. Pub. No. WO00/62339, published Oct. 10, 2000. Ex. 1008 (English translation).

[7] Steve Trimberger, Dean Carberry, Anders Johnson, and Jennifer Wong, *A Time-Multiplexed FPGA*, Proceedings of the 1997 IEEE International Symposium on Field-Programmable Custom Computing Machines, April 1997, ISBN 0-8186-8159-4. Ex. 1006.

Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. *Level of Ordinary Skill in the Art*

Relying on the testimony of Dr. Franzon, Petitioner contends that

> [t]he person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '226 patent would have been a person with a Bachelor's Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication.

Pet. 5 (citing Ex. 1002 ¶¶ 58–60).

Patent Owner asserts that

> [a] person of ordinary skill in the art ("POSITA") around December 5, 2001 (the earliest effective filing date of the '226 Patent) would have had a Bachelor's degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.

PO Resp. 10 (citing Ex. 2006 ¶ 25).

As we did in the Decision on Institution, we adopt Petitioner's proposed level of ordinary skill in the art, which comports with the teachings of the '226 patent and the asserted prior art. *See* Dec. on Inst. 21. Patent Owner's proposed level overlaps substantially with Petitioner's proposed level. Even if we adopted Patent Owner's proposed level, the outcome would remain the same.

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner and Patent Owner each agree that both "means for reconfiguring the programmable array within one clock cycle" (limitation in claim 13) and "means for updating the plurality of configuration logic cells within one clock cycle" (limitation 22.4 in claim 22) are means- plus-function limitations and should be construed as per 35 U.S.C. § 112, ¶ 6. Pet. 10–13; PO Resp. 11.

Both of these limitations listed above recite "means" and further recite a function, thus creating a presumption that 35 U.S.C. § 112, ¶ 6 applies. *See* 35 U.S.C. § 112, ¶ 6 ("An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and

such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."); *see also Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (en banc in relevant part) (quoting *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 703 (Fed. Cir. 1998)) (holding that "use of the word 'means' creates a presumption that § 112, ¶ 6 applies"). We agree with the parties that these limitations are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6. Pet. 11, 13; PO Resp. 11.

Patent Owner additionally argues that we should construe "wide configuration data port," which appears in challenged claims 14 and 23, and which additionally appears in each party's proposals for the structure of the means-plus-function limitations described above. Pet. 11–13; PO Resp. 19– 25; Pet. Reply 2–6; PO Sur-reply 1–5. Because of this, we begin with this construction and then discuss construction of the means-plus-function terms.

1. *"wide configuration data port"*

While neither party proposed construction of this term in pre- institution briefing, Patent Owner did propose its construction in its Response, and the parties each briefed the construction before the oral hearing. PO Resp. 14–20; Pet. Reply 3–6; PO Sur-reply 1–5.

a. Patent Owner's Position

Patent Owner argues that the term "wide configuration data port" should be construed as "a configuration data port that allows the parallel updating of logic cells in a programmable array

through use of buffer cells." PO Resp. 15–19 (citing Ex. 1001, 4:45–59, Fig. 5; Ex. 2006 ¶¶ 32, 40–44); In support of this construction, Patent Owner cites as intrinsic evidence the '226 patent's disclosure that the wide configuration data port "is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cells 88." Ex. 1001, 4:51–54 (quoted at PO Resp. 15). Patent Owner argues that the '226 patent describes, as background and in contrast to the use of a wide configuration data port, the use of a "relatively narrow" serial data port that accesses configuration memory serially. *Id.* at 17–19 (citing Ex. 1001, 3:63–4:9, Fig. 5; Ex. 2006 ¶¶ 42–44).

Patent Owner contends that the '226 patent disclosure distinguishes the wide configuration data port because it allows the updating of logic cells in parallel through use of buffer cells, which Patent Owner argues is "a key distinguishing feature of the wide configuration data port." *Id.* at 18–19. Patent Owner argues that its experts "have been consistent that the word 'wide' in this term requires a sufficient number, and appropriate arrangement, of connections between the memory die and the programmable array to permit parallel updating of the array." PO Sur-reply 2 (citing Ex. 2006 ¶ 38; Ex. 1076, 42:3–20). Patent Owner argues that the buffer cells must be part of a proper construction. Patent Owner contends that "the wide configuration data port 82 achieves single cycle reconfiguration of the programmable array *by loading reconfiguration data into buffer cells 88 in parallel*, even while the programmable array is operational." PO Resp. 16 (emphasis added). In the Sur-reply, however, Patent Owner contends that it is not the parallel loading of reconfiguration data into

buffer cells that allows single cycle reconfiguration, but rather the updating of the logic cells in parallel, using the data in the buffer cells. PO Sur-reply 4–5. Patent Owner further supports its contention that the buffer cells must be included with the die- area connections in the construction of "wide configuration data port" because "Petitioner fails to point to any embodiment in the '226 Patent in which the vertical die-area connections and the buffer cells are not used in conjunction and therefore cannot credibly claim that Arbor's construction excludes such an embodiment." *Id.* at 3.

b. Petitioner's Position

Petitioner, in its Reply, argues that the term should have its plain and ordinary meaning. Pet. Reply 3–4. Petitioner argues that the plain and ordinary meaning of a configuration data port is "a port for configuration data, i.e., a connection or place through which configuration data is transferred." *Id.* (citing Ex. 1002 ¶¶ 96–97; also citing Ex. 1075, 163:8–163:21 (deposition of Patent Owner's expert Dr. Krishnendu Chakrabarty in the 1022IPR)). Petitioner argues that the '226 patent shows a configuration data port that is wide because it includes direct connections / paths for configuration data to be loaded, contrasting this with the Figure 3 prior art embodiment of the '226 patent, which is not "wide." *Id.* at 3–4 (citing Ex. 1002 ¶¶ 96–97).

With respect to Patent Owner's proposed construction, Petitioner argues that Arbor's proposal improperly includes the buffer cells, which are shown and described in the '226 patent as separate elements from the wide configuration data port. *Id.* at 4 (citing Ex. 1001, 4:50–54, Fig. 5). Petitioner argues that the

construction is contradicted by testimony presented by Patent Owner's expert Dr. Chakrabarty in the 1022IPR, and that Dr. Souri did not read this testimony. *Id.* at 5 (citing Ex. 1076, 73:22–74:7). Petitioner argues Patent Owner's construction, in its use of the term "allows," is ill-defined, and that Patent Owner describes elements such as logic cells, configuration memory, and a large number of die-area contacts as required, but that these elements are not included in the proposed construction. *Id.* at 4–5. Lastly, Petitioner argues that Patent Owner incorrectly asserts that the loading of reconfiguration data into buffer cells occurs in one clock cycle, but that it is the updating of the logic cells that occurs in one clock cycle in the '226 patent. *Id.* at 6 (citing PO Resp. 16; Ex. 1001, 4:55–59; Ex. 1070 ¶ 111).

c. Analysis and Conclusion

We determine that one of ordinary skill in the art would not understand the ordinary and customary meaning of "wide configuration data port" to include buffer cells or configuration memory cells, and construction in accordance with the prosecution history would likewise not require the inclusion of buffer cells or configuration memory cells. We also note that Patent Owner's proposed construction ("a configuration data port that allows the parallel updating of logic cells in a programmable array through use of buffer cells") contains some ambiguity in not making clear how buffer cells *allow* parallel updating, and we decline to provide a construction including this ambiguity.

The '226 patent does not make extensive use of the term "wide configuration data port." With the exception of the claims, which do not provide

additional context, the references in the '226 patent are the labelling of element 82 of Figure 5 as "very wide configuration data port" and the paragraph referencing this figure, cited extensively by both parties, in which the specification describes the following:

> With reference additionally now to FIG. 5, a corresponding functional block diagram of the configuration cells 80 of the reconfigurable processor module 60 of the preceding figure is shown wherein the FPGA 70 may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel. As opposed to the conventional implementation of FIG. 3, a wide configuration data port 82 is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cell 88. The buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4). In this manner, they can be loaded while the FPGA 68 comprising the logic cells 84 are in operation. This then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it configuration logic cells 84 updated in parallel. Other methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory ("RAM") than can be offered within the FPGA die 68 itself.

Ex. 1001, 4:45–65 (cited or quoted in whole or part at PO Resp. 15–16; Pet. Reply 4, 6; PO Sur-reply 3–5).

Patent Owner, in focusing on this portion of the '226 patent disclosure, does not adequately explain why buffer cells and configuration memory cells must be included in the proper construction of "wide configuration data port," and seeks to import a functional description of the use of a wide configuration data port ("that *allows parallel updating* of logic cells in a programmable array through use of buffer cells") into the claim construction. PO Resp. 15–17; PO Sur-reply 2–4. While the discussion in the '226 patent describes an example of a wide configuration data port used in a specific way that aligns with Patent Owner's proposal (Ex. 1001, 4:45– 59), other examples of the use of a wide configuration data port are included (*id.* at 4:59–65), and therefore we do not agree that one of ordinary skill would understand this use to be part of the construction of the term.

We agree with Petitioner that the proper construction of the term does not require buffer cells. *See* Pet. Reply 4–6. Rather, we note that the specification of the '226 patent contrasts loading of data to an FPGA in a byte serial fashion through a narrow port, which "results in [] long reconfiguration times," with the use of a wide configuration data port, and therefore we determine that one of ordinary skill would understand the wide configuration data port, in contrast to the byte serial "relatively narrow" port, to include parallel connections between cells in the dies. *See* Ex. 1001, 4:3–9. This additionally is consistent with certain arguments by Patent Owner, for example in the Patent Owner's Response, which opens with a discussion of the "innovative" processor's arrangement of die-area contacts, such as through-silicon vias, "into a wide configuration data port" and

we find that description more consistent with the proper construction of this term. PO Resp. 1–2; *see also* PO Sur-reply 2–3 ("Arbor's experts have been consistent that the word 'wide' in this term requires a sufficient number, and appropriate arrangement, of connections between the memory die and the programmable array to permit parallel updating of the array.")

In the Final Written Decision issued in the 1022IPR, we construed "wide configuration data port" to be "a configuration data port connecting in parallel cells on one die element to cells on another die element." IPR2020- 01022, Paper 34 at 13–16 (PTAB Nov. 24, 2021). During the hearing, we referred to that decision, indicated our interest in the Petitioner's and Patent Owner's positions on its claim constructions, and the parties discussed our constructions in that proceeding to some degree in their arguments. Tr. 6:1– 6, 25:12–30:6, 43:6–23, 61:18–63:10.

The '226 patent describes updating the logic cells of an FPGA in one clock cycle to reconfigure the FPGA by loading associated configuration memory from buffer cells, preferably located on a different die element. Ex. 1001, 4:45–59. Additionally, the '226 patent describes that doing this "takes advantage of the significantly increased number of connections to the cache memory die." *Id.* at 4:59–65. This construction is supported by Petitioner's expert's description of the plain and ordinary meaning of "configuration data port" as "a connection or place through which configuration data is transferred" and that in the prior art wide buses were made possible by 3-D stacking. *See, e.g.*, Ex. 1002 ¶¶ 54, 96–97. This

construction additionally is supported by Patent Owner's expert's description that "the inventors of the '226 Patent arranged die-area contacts of the SDH [(stacked die hybrid)] processor, such as through-silicon vias ('TSVs'), into a wide configuration data port that reconfigures them in a parallel scheme." Ex. 2006 ¶ 32; *see also* PO Resp. 1–2; PO Sur-reply 4–5 ("the wide configuration data port . . . includes a large number of die-area interconnections (*e.g.*, TSVs) that interconnect stacked chips"); Ex. 1075, 157:23–158:3, 163:8–163:21 (Patent Owner's expert in the 1022 IPR). The specification supports a construction of the wide configuration data port as a configuration data port that makes connections between die elements in parallel. Ex. 1001, 3:33–37, 4:45–65; *see also id.* at code (57) ("significant acceleration in the sharing of data between the microprocessor and the FPGA element").

The '226 patent describes the loading of buffer cells, preferably on the memory die, while the programmable array is in operation, with the configuration logic cells then updated in parallel from the buffer cells through the significantly increased number of connections for reconfiguration in one clock cycle. Ex. 1001, 4:45–59. But none of the challenged claims requires configuring or updating while the programmable array/FPGA is in operation. And the specification shows that the buffer cells are not part of the wide configuration data port. *See id.* at Fig. 5. They are described, rather, as preferably part of the memory die. *Id.* at 4:54–55. We determine that the specification supports a construction that the parallel connection between die elements are between cells on each die element. This parallel connection implies that cells on one die are connected in parallel to cells

on another die, for example, buffer cells or configuration memory cells. *Id.* at 4:50–55, Fig. 5.

For these reasons, we construe "wide configuration data port" as "a configuration data port connecting in parallel cells on one die element to cells on another die element."

2. *Limitation 13.4 – "means for reconfiguring the programmable array within one clock cycle"*

The first step in construing a means-plus-function claim element is to identify the recited function in the claim element. *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003). The second step is to look to the specification and identify the corresponding structure for that recited function. *Id.*

Petitioner argues that the recited function for limitation [13.4] is "reconfiguring the programmable array within one clock cycle." Pet. 11. Patent Owner agrees. PO Resp. 11. We also agree. *See Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999) ("[35 U.S.C. § 112, ¶ 6] does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.")

We next review the '226 patent to determine the corresponding structure for the identified function. Our preliminary determination in the Decision on Institution was that the correct corresponding structure would be "a wide configuration data port interconnecting a memory and the programmable array using contact points distributed through the first integrated circuit die element and the third

integrated circuit die element." Dec. on Inst. 23–29. In the Final Written Decision in the 1022 IPR, we determined that the correct corresponding structure is "a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element." IPR2020-01022, Paper 34 at 17–21; *see* Tr. 6:1–6, 25:12–30:6, 43:6–23, 61:18–63:10 (raising and/or discussing constructions from the Final Written Decision in the 1022 IPR).

In the Petition, Petitioner proposed two structures from the '226 specification as the corresponding structure: "a wide configuration data port [used] to update the various logic cells through an associated configuration memory and buffer cell" and "a stacked FPGA die and memory die interconnected by a wide configuration data port using contact points distributed throughout the dies." Pet. 11–13. In Reply, Petitioner agrees with our preliminary determination, but in the alternative refers to the two structures discussed in the Petition. Pet. Reply 2.

Patent Owner proposes that the structure is simply a "wide configuration data port," according to its construction of that term, which includes buffer cells. PO Resp. 11–20; PO Sur-reply 5 ("[T]he buffer cells connected in parallel (using die-area interconnections) with the memory configuration cells allow for FPGA to be totally reconfigured in one clock cycle."). Patent Owner contends that what allows for the reconfiguration in one clock cycle is "buffer cells connected in parallel . . . with the memory configuration cells" "using die-area connections." PO Sur-reply 5.

"While corresponding structure need not include all things necessary to enable the claimed invention to work, it must include all structure that actually performs the recited function." *Default Proof Credit Card Sys. Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). Conversely, structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations. *Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc.*, 145 F.3d 1303, 1308–09, (Fed. Cir. 1998); *see B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997) ("[S]tructure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.").

Patent Owner's arguments regarding buffer cells connected with memory configuration cells using die-area interconnections requires that the buffer cells be located on a different die than the memory configuration cells, but the '226 patent discloses only that "[t]he buffer cells 88 are preferably a portion of the memory die 66" and not that they always are on the memory die, and also that the significantly increased number of connections to the cache memory die may allow the cache memory die to replace configuration bit storage on the FPGA die. Ex. 1001, 4:50–54, 4:59–63. Thus, we decline to require in the corresponding structure that buffer cells or configuration memory are included on any die element.

Rather, we find that what is disclosed as actually performing the recited function of "reconfiguring the

programmable array within one clock cycle" is "a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element." The support for this is found in the '226 patent's comparison of the long reconfiguration times through a narrow port (Ex. 1001, 4:3–9) with the time to reconfigure through a wide configuration data port with a significantly increased number of connections (*id.* at 4:45– 65), and the implementation of this in a module that has multiple dies "which have a number of corresponding contact points, or holes, 70 formed throughout the area of the [die] package" (*id.* at 4:9–20). The use of a wide configuration data port, as per our construction, implicates two die elements. This was reflected in our preliminary claim construction, for which the corresponding structure described "contact points distributed through the first integrated circuit die element and the third integrated circuit die element." Dec. on Inst. 29. As the function is "reconfiguring the programmable array within one clock cycle," one of the die elements is the first integrated circuit die element, which includes the programmable array.

We acknowledge that, in the Samsung litigation, the District Court for the Eastern District of Texas has construed this limitation (and limitation 22.4). Ex. 2005.[8] The District Court construed the function

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[8] We additionally acknowledge the construction for certain additional limitations in the challenged claims, which the parties do not address construction of, and which we do not herein construe. Ex. 1036, 18–25 ("processor module"), 25–37 ("programmable array"), 38–44 ('stacked with and electrically coupled to"), 44–49 ("contact points distributed throughout the surfaces of said die elements"). However, the patentability

for this limitation identically, and the corresponding structure as "wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof." *Id.* at 8–18. The chief distinction between this construction and the one that we adopt is the inclusion of all die elements in the District Court claim construction, rather than only the first die element (including the programmable array) and one additional die element in ours. Our patentability determination here would be the same were we to adopt the construction provided by the District Court for the corresponding structure of the means-plus-function limitations.

For the reasons discussed above, we determine that, for means-plus- function limitation 13.4 of claim 13, the function is "reconfiguring the programmable array within one clock cycle," and the corresponding structure is "a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element."

3. *Limitation 22.4 – "means for updating the plurality of configuration logic cells within one clock cycle"*

Petitioner and Patent Owner refer back to or recapitulate their arguments with respect to limitation 13.4 in their arguments for the function and structure of means-plus-function claim limitation 22.4. Pet. 13; PO Resp. 11–20; Pet. Reply 2; PO Sur-reply 5. To support arguments regarding this claim

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determination here would be the same were we to explicitly adopt the construction provided by the District Court for those terms.

term, the parties cite no additional disclosure other than that previously discussed, and we agree that the previously discussed disclosure supports the construction of claim limitation 22.4. Claim 22 differs from claim 13 in several respects, including the inclusion of a plurality of configuration logic cells in the first integrated circuit die element. Limitation 22.4 differs from limitation 13.4 in its statement of function ("updating the plurality of configuration logic cells" rather than "reconfiguring the programmable array"). The configuration logic cells referenced are included in the first integrated circuit die element, and thus here too, the corresponding structure specifies the first integrated circuit die element is included in the description of the structure. Ex. 1001, 8:4–17.

For the reasons presented above, we find that, for means-plus-function limitation 22.4 of claim 22, the function is "updating the plurality of configuration logic cells within one clock cycle," and the corresponding structure is "a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element."

4. *Limitation 1.3 –"such that processing of data shared between the microprocessor and the field programmable gate array is accelerated"*

While neither party explicitly requests construction of this claim limitation, certain of the arguments presented by the parties relate to their different understandings of this limitation.

Patent Owner presents arguments indicating that it interprets "data shared between the

microprocessor and the field programmable gate array" in limitation 1.3 to require more than data being transferred from the microprocessor to the FPGA. PO Resp. 30–36; PO Sur-reply 7–8. Patent Owner argues that a showing by Petitioner that the output data of a microprocessor is sent to the FPGA would not satisfy this limitation, because no data is described as being processed by both the microprocessor and the FPGA. PO Resp. at 31–32 (citing Ex. 2006 ¶ 65); PO Sur-reply 7–8. Patent Owner argues that the '226 patent explicitly describes memory that is equally accessible by both a microprocessor and an FPGA with equal speed, asserting that this too is required. PO Resp. 34–36 (citing Ex. 1001, 4:34– 44; Ex. 2006 ¶ 69); PO Sur-reply 7–8 (citing Ex. 1001, 1:62–2:3, 2:50–54, 4:34–44; Ex. 2006 ¶ 69). Patent Owner's expert quotes the description of the embodiment in Figures 4 and 5 of the '226 patent as including a memory "accessible by both the microprocessor 64 and the FPGA 68 with equal speed" and indicates that the "references fail" because they do not provide data shared between an FPGA and a microprocessor and accessible to each with "anything approximating 'equal speed.'" Ex. 2006 ¶¶ 69–70.

Petitioner argues that "there is no reasonable argument that data transferred back and forth between the processor and the programmable array is not being shared between them" and that Patent Owner's arguments improperly exclude direct sharing of data between the microprocessor and the FPGA. Pet. Reply 7–8 (citing Ex. 1001, code (57), 2:50–54; Ex. 1070 ¶¶ 73–74).

We agree with Petitioner that this limitation does not require a memory accessible by both a microprocessor and FPGA with equal speed, or that the same data be processed by both the microprocessor and the FPGA. While Patent Owner is correct that the '226 patent describes the stacking of a memory die in between a processor die and an FPGA die in the embodiment of Figures 4 and 5, no memory die is claimed or mentioned in claim 1. Additionally, claim 2, which depends from claim 1 and further requires a memory IC die element, requires only that that memory IC die element be connected to one or the other of the FPGA IC die element or the microprocessor IC die element of claim 1. Ex. 1001, 6:27–32. The'226 patent specification describes one embodiment in which memory on a cache memory die is accessible by a microprocessor and FPGA with equal speed; however, we do not read this requirement into claim 1, which does not require a memory IC die element. *See id.* at 4:34–39.

Additionally, the'226 patent specification provides no support for Patent Owner's contention that the same data must be processed by the microprocessor and the FPGA or any description of this occurring. The specification describes "accelerating the sharing of data between the microprocessor and the FPGA." Ex. 1001, code (57), 2:50–57. The specification additionally presents instances in which data is transferred from one element to the other and processed/used by the recipient after the transfer, for example, the use of transferred data to reconfigure the FPGA, and the FPGA providing test stimulus for the microprocessor during manufacturing. *Id.* at 4:34–65, 5:5–15. Each of these describes only sharing of data from one die

component to another, and not equal accessibility or any mutual processing of the same data.

Therefore, while we do not provide an explicit construction of "such that processing of data shared between the microprocessor and the field programmable gate array is accelerated," we determine that the correct construction does not require a memory that is equally accessible by the microprocessor and the field programmable gate array, that the correct construction does not require that some data be processed by both the microprocessor and the field programmable gate array, and that the correct construction does not require data to be accessed at equal or approximately equal speed by the microprocessor and the field programmable gate array.

5. *No additional constructions*

No other terms require explicit construction. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'. . . ." (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness, Claims 1–6*

Petitioner contends the subject matter of claims 1–6 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 14–41. Patent Owner disputes Petitioner's contentions. PO Resp. 30–44.

1. *Zavracky*

Zavracky describes "a multi-layered structure" including a "microprocessor . . . configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure." Ex. 1003, code (57). Zavracky's "invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing." *Id.* at 2:5–10. Zavracky includes numerous types of stacked elements, including "programmable logic devices" (PLDs) stacked with "memory" and "microprocessors." *See id.* at 5:19–23.

Zavracky's Figure 12 follows:

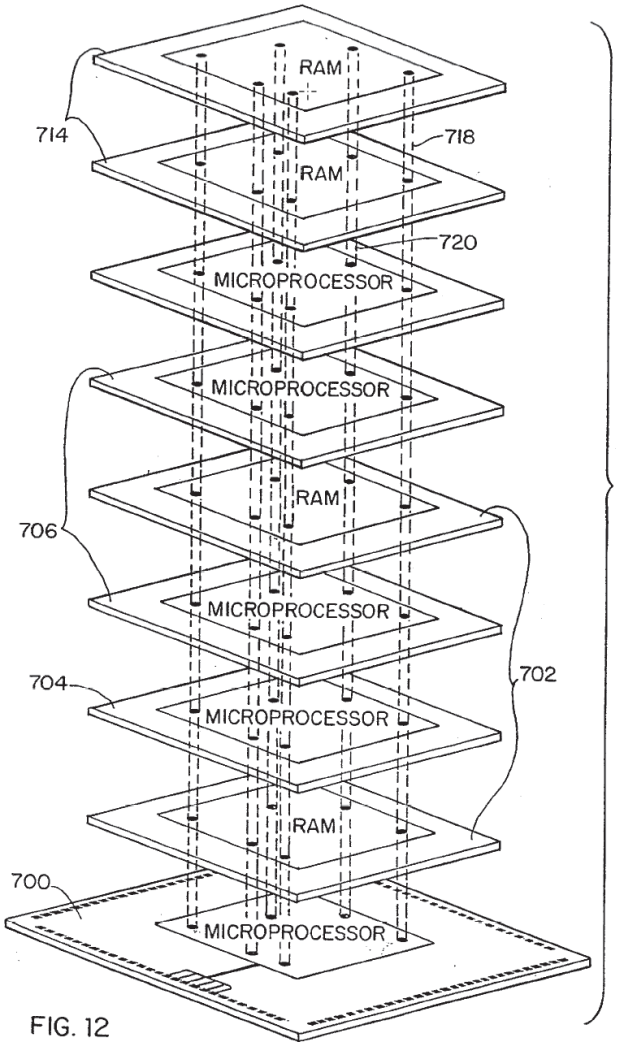

FIG. 12

Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements wherein "buses run vertically through the stack by the use of inter-layer connectors." Ex. 1003, 12:24–26.

2. *Chiricescu*

Chiricescu describes a three-dimensional chip, comprising an FPGA, memory, and routing layers. Ex. 1004, 1. Chiricescu's FPGA includes a "layer of on-chip random access memory . . . to store configuration information." *Id.* Chiricescu describes and cites the published patent application that corresponds to Zavracky as follows:

> At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.

See id. at 1, 4 (citing "M. P. Zavracky, Zavracky, D-P Vu and B. Dingle, '*Three Dimensional Processor using Transferred Thin Film Circuits*,' US Patent Application # 08-531-177, allowed January 8, 1997").[9] Chiricescu describes "[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information." Ex. 1004, 1. Chiricescu also describes using memory on-chip to "significantly improve[] the reconfiguration time," explaining as follows:

> The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to

[9] Zavracky lists the same four inventors and "Appl. No. 531,177," which corresponds to the application number cited by Chiricescu. Ex. 1003, codes (75), (21).

manage cache memory can be used to administer the configuration data.

Id. at 3.

Figure 2 of Chiricescu follows:

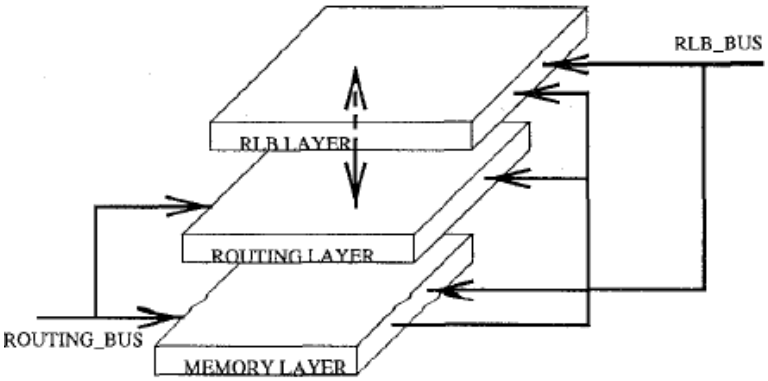

Figure 2. The layers of our 3-D FPGA architecture.

Figure 2 illustrates three layers in the 3D-FPGA architecture, with the RLB layer including routing and logic blocks in in a "sea-of-gates FPGA architecture," a routing layer, and the aforementioned memory layer (to program the FPGA). *See* Ex. 1004, 1–2.

3. *Akasaka*

Akasaka, a December 1986 paper published in the Proceedings of the IEEE, generally describes trends in three-dimensional integrated stacked active layers. Ex. 1005, 1. Akasaka states that "tens of thousands of via holes" allow for parallel processing in stacked 3-D chips, and the "via holes in 3-D ICs" decrease the interconnection length between IC die elements so that "the signal processing speed of the

system will be greatly improved." *Id.* at 3. Akasaka further explains that "high-speed performance is associated with shorter interconnection delay time and parallel processing" so that "twice the operating speed is possible in the best case of 3-D ICs." *Id.*

Also, "input and output circuits . . . consume high electrical power." Ex. 1005, 3. However, "a 10-layer 3-D IC needs only one set of I/O circuits," so "power dissipation per circuit function is extremely small in 3- D ICs compared to 2-D ICs." *Id.*

Figure 4 of Akasaka follows:

Fig. 4. Wiring for parallel processing in 2-D and 3-D ICs.

Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

4. *Claim 1*

For its arguments that claim 1 is unpatentable, Petitioner relies on a combination of Zavracky, Chiricescu, and Akasaka, "integrat[ing]" Zavracky's "stacked interconnected programmable 3-D module," Chiricescu's "accelerated FPGA reconfiguration using stacked memory," and Akasaka's "thousands of distributed interconnections." Pet. 18.

a. Combination of Zavracky, Chiricescu, and Akasaka

With respect to the combination of Zavracky and Chiricescu, Petitioner argues that Chiricescu explicitly references and uses the interconnections of Zavracky. Pet. 18 (citing Ex. 1002 ¶¶ 218–232); *see* Pet. 16 & n.3; *supra* § II.D.2 (noting the explicit citation to and description of Zavracky in Chiricescu). Petitioner further argues that one of ordinary skill would have used Chiricescu's teachings with Zavracky's 3-D stacks to achieve improvements in reconfiguration time. *Id.* at 18–19 (citing Ex. 1002 ¶¶ 221–228 (citing Ex. 1004, 2; Ex. 1003, 5:65–66)). Additionally, Petitioner argues that the combination would have been motivated by Chiricescu's suggestion of using an FPGA for "arbitrary logic functions" to "expand" on the limited task performed by the programmable logic device in Zavracky, to combine prior art elements according to known methods to yield a predictable result, and as a routine modification. Pet. 19–20 (citing Ex. 1003, 2:29–39; Ex. 1004, 1; Ex. 1002 ¶¶ 229–232).

Petitioner argues that the further combination of Akasaka with Zavracky and Chiricescu would have been motivated by a desire to increase bandwidth and processing speed through better parallelism and increased connectivity. Pet. 20 (citing Ex. 1005, 3; Ex. 1002 ¶ 233). Petitioner contends that Zavracky and Chiricescu each teach or suggest that connections could be placed anywhere on the die. *Id.* (quoting Ex. 1003, 6:43–47; citing Ex. 1004, 1). To improve Zavracky's stacks, according to Petitioner, one of ordinary skill would have sought out Akasaka's teachings to increase bandwidth and processing speed

and expected success. *Id.* (citing Ex. 1002 ¶ 235). Petitioner also argues that Akasaka's communication structure would have enabled desirable uses of the Zavracky-Chiricescu combination. *Id.* at 20–21 (citing Ex. 1005, 11, Fig. 25; Ex. 1002 ¶¶ 236–237). Petitioner also argues that one of ordinary skill would have been motivated to make a combination with Akasaka, and that such a combination "would have been a logical extension" to the Zavracky- Chiricescu combination, in light of "many references teaching stacked dies with thousands of distributed connections." *Id.* at 21 (citing Ex. 1009; Ex. 1030; Ex. 1021; Ex. 1002 ¶¶ 238–239).

Patent Owner argues that one of ordinary skill in the art would not have combined Zavracky, Chiricescu, and Akasaka as Petitioner argues. PO Resp. 36–44.

Patent Owner argues that, because Chiricescu discloses configuration data stored in on-chip memory, the combination of Chiricescu and Zavracky would result in a structure in which data is removed from the microprocessor's cache to be stored in the FPGA's on-chip memory, which would make the data harder for the microprocessor to access. PO Resp. 37–38. This is based on Patent Owner's argument that Zavracky and Chiricescu both include only a small number of vertical interconnections between the layers. *Id.*; *see id.* at 20 (describing Zavracky as disclosing a small number of vertical interconnections between layers), 26 (describing Chiricescu as having only a small number of interconnects between memory and RLB layers).

Patent Owner additionally argues that the combination of Zavracky and Chiricescu would not

have resulted in the acceleration of data shared between a microprocessor and an FPGA. *Id.* at 38–39. Patent Owner calls the motivation to combine "untethered to the accelerating processing claims," in an argument relating to its interpretation of limitation 1.3, discussed above at Section II.C.4. *Id.* at 38–39 (citing Ex. 2006 ¶ 75 (Dr. Souri's testimony describing the reasons for combining as flawed because "none of the cited references disclose the processing of shared data" or acceleration of such processing)). Lastly, Patent Owner argues that major modifications would need to be made to the combination of Zavracky and Chiricescu to allow for the accelerated processing of shared data, again, relating to Patent Owner's interpretation of limitation 1.3 of claim 1. *Id.* at 38–41.

With respect to the combination of Zavracky, Chiricescu, and Akasaka, Patent Owner argues, again with reference to its interpretation of limitation 1.3 of claim 1, that Akasaka does not remedy the issues it argues are present with a combination of Zavracky and Chiricescu with respect to accelerating the processing of shared data. *Id.* at 41–42. Citing Figure 25 of Akasaka, Patent Owner argues that Akasaka teaches each processor in a stack only accessing memory in its own layer. *Id.* at 41–42. Again referencing Figure 25 of Akasaka, Patent Owner argues that Petitioner "does not attempt to adequately explain ***how*** a POSITA would incorporate Akasaka's common memory data system into the combined Zavracky- Chiricescu system to achieve accelerated processing of data shared between a microprocessor and an FPGA." *Id.* at 42. Patent Owner argues that Akasaka's Figure 25 teaches that "each individual processor disclosed in Akasaka only

has direct access to its own memory and not any other processor's memory." PO Sur-reply 9.

Patent Owner argues that the modification of Zavracky-Chiricescu with Akasaka would require the stacked memory from Chiricescu to be moved to its FPGA layer, which would be contrary to Chiricescu's principle of operation that moves memory out of the FPGA layer. *Id.* at 43–44.

Patent Owner's arguments are unavailing. To the extent that they rely on Patent Owner's construction of limitation 1.3, the arguments fail as we have not adopted this construction. *See supra* § II.C.4. Additionally, Petitioner's arguments regarding a "common data memory" and citations to Akasaka's Figure 25 relate to the knowledge of one of ordinary skill for "common data memory" and not to any indication that the specific configuration of Figure 25 would be used in the combination. *See* Pet. 20– 21, 30–31. As Petitioner discusses, Zavracky specifically describes a stacked configuration of integrated circuit elements, and connecting bus lines between an FPGA/PLD element and other integrated circuit elements, including memory and a processor. *See* Pet. 14–15, 23–24 (citing Ex. 1003, 2:5–10, 3:62–4:4, 4:7–9, 5:19–23, 6:43–47, 12:12–38, 14:56–58, Figs. 12, 13). Petitioner shows a number of other stacked dies or layers with multiple via connections – in addition to Akasaka (Ex. 1005, Fig. 4), Petitioner cites Franzon (Ex. 1020, Fig. 4), Koyanagi (Ex. 1021, Fig. 1(a)), and Alexander (Ex. 1028, Fig. 2(g)). *See id.* at 21, 37. As discussed further below, Trimberger (Ex. 1006) also shows parallel loading by "*flash reconfiguring* all [100,000] bits in logic and interconnect array [i.e., an FPGA] . . . simultaneously from one memory plane."

Ex. 1006, 22.[10] Patent Owner concedes Zavracky and Chiricescu each show how to connect layers with a small number of vertical interconnections. PO Resp. 20 (Zavracky), 26 (Chiricescu), 38. Petitioner shows that a large number of vias would have been obvious in view of the combined teachings, to enhance speed, allow parallel processing and data transfer, minimize latency, and maximize bandwidth.

Thus, Petitioner persuasively relies on the knowledge of the artisan of ordinary skill and the combined teachings of Zavracky, Chiricescu, and Akasaka supported by specific reasons and rational underpinning to show how the combination teaches or suggests increasing the number of contact points or via holes for electrically coupling FPGA, memory, and processors together. Petitioner also shows the "why"––to allow for parallel data transfers, speed increases, larger bandwidth, etc., all with a reasonable expectation of success.

b. Preamble, Limitation 1.1, and Limitation 1.2

Claim 1's preamble recites "[a] processor module comprising." Petitioner relies on the combined teachings of Zavracky, Chiricescu, and Akasaka, as discussed further below, and provides evidence that Zavracky discloses a processor module, including a programmable array, memory (RAM), and microprocessor as part of a stack of dies forming a 3-D device. *See* Pet. 22 (reproducing Ex. 1003, Figs. 12–

[10] Petitioner employs Trimberger to address challenged claims 13–30 as discussed further below (§ II.F), but it is also further evidence of a reasonable expectation of success as it relates to connecting several thousands of bit lines in parallel.

13; citing Ex. 1003, 2:1–7, 5:19–23, 9:42–45, 12:12–38, Figs. 12–13; Ex. 1002 ¶¶ 282–288).

Claim 1 recites limitation 1.1, "at least one field programmable gate array integrated circuit die element including a programmable array." Petitioner contends that the combined teachings of Zavracky and Chiricescu render the limitation obvious. Pet. 23–24. Petitioner relies on Zavracky's layers as teaching dies, citing Zavracky's description of interlayer connections as "placed anywhere on the die" and thereby "achieved with a minimal loss of die space." *Id.* (quoting Ex. 1003, 6:43-7:9; citing Ex. 1003 4:63–65, 10:61–65, Figs. 1 (element 140), 6, 7; Ex. 1002 ¶¶ 278–280). Thus, Petitioner argues that Zavracky describes stacked layers of integrated circuit die elements. *Id.* at 24. Petitioner further argues, with reference to PLD 802 in Figure 13 of Zavracky and its described programming to provide a user-defined communication protocol, that one of ordinary skill in the art would have understand that an FPGA was an example of such a programmable logic device. *Id.* at 24–25 (citing Ex. 1003, 5:21–23, 12:33–36, Fig. 13; Ex. 1002 ¶¶ 293–295). Petitioner adds that, Chiricescu describes Zavracky as teaching technology "to build 3-D layered FPGAs" and thus confirms the understanding of Zavracky as teaching an FPGA. *Id.* at 25 (citing Ex. 1004, 1; Ex. 1002 ¶ 296). Additionally, in a combination of Chiricescu and Zavracky, Petitioner contends that Chiricescu's "sea-of-gates FPGA" would teach or suggest an FPGA as the PLD layer of Zavracky. *Id.* (citing Ex. 1004, 1, 3).

With respect to the "programmable gate array" of limitation 1.1, Petitioner first refers to its arguments with respect to an FPGA as the PLD, asserting that

the FPGA includes a programmable array. *Id.* at 25–26 (citing Ex. 1002 ¶ 288). Next, Petitioner argues that in the combination of Chiricescu and Zavracky, the configurable routing and logic blocks in the FPGA layer teaches a programmable gate array. *Id.* at 26 (citing Ex. 1004, 1; Ex. 1002 ¶ 299).

Petitioner argues that the "microprocessor integrated circuit die element" of limitation 1.2 is taught in Zavracky's layered multi-processor system (Figure 12) or multi-layer microprocessor (Figure 13), citing the multiple multiprocessors, each on one die element in the Figure 12 embodiment, and the multi-layer microprocessor in the Figure 13 embodiment. Pet. 27–28 (citing Ex. 1003, Fig. 12 (elements 700, 704, 705), Fig. 13 (elements 804, 806); Ex. 1002 ¶¶ 310–312). Limitation 1.2 further requires that this die element be "stacked with an electrically coupled" to the programmable array of the die element from limitation 1.1. Petitioner cites Zavracky's teaching of vertically stacked and interconnected circuit element layers, electrically coupled to each other. *Id.* at 28 (citing Ex. 1003, 2:7–8, 11:63–12:2, 12:13–39, 14:51–63).

Other than addressing motivation as discussed herein, Patent Owner does not make any specific arguments with respect to these limitations.

c. Limitation 1.3 of Claim 1

With respect to the final limitation 1.3 of claim 1, "such that the processing of data shared between the microprocessor and the field programmable gate array is accelerated," Petitioner argues that Zavracky's programmable logic acting as an intermediary to the microprocessor means that data

is shared between the microprocessor and programmable logic. Pet. 29 (citing Ex. 1003, 12:28–38; Ex. 1002 ¶ 342). Petitioner further argues that Akasaka's thousands of via holes would have been used to allow information to be transferred between die layers. *Id.* at 30 (citing Ex. 1005, 3; Ex. 1002 ¶¶ 233–239, 347–348).

To teach or suggest "that processing . . . is accelerated" as per limitation 1.3, Petitioner argues that Zavracky's approach offers higher speed from "reduction in the length of the busses." Pet. 30 (quoting Ex. 1003, 3:1–11; citing Ex. 1002 ¶ 346). Petitioner additionally cites Akasaka's teaching of "thousands of via holes" to permit parallel processing, and that "twice the operating speed is possible in the best case of 3-D ICs." *Id.* at 17, 31 (quoting Ex. 1005, 3 (emphasis omitted); citing Ex. 1002 ¶ 347). Additionally, Petitioner cites similar teachings of Chiricescu with respect to benefits from a stacked arrangement with vertical interconnects and the background knowledge of one of ordinary skill in the art. *Id.* at 5– 10, 17 (citing Ex. 1004, 3; Ex. 1002 ¶ 348).

Patent Owner contends that the Zavracky-Chiricescu-Akasaka combination does not teach or suggest limitation 1.3's feature of accelerating processing of data. PO Resp. 30–36. Patent Owner argues that Petitioner only describes data being transferred from a microprocessor to an FPGA, and not shared. *Id.* at 31–32. Patent Owner contends that "***data processed*** by *Zavracky's* microprocessor is not even shared with the FPGA" but rather that "it is the ***output*** of *Zavracky's* microprocessor that is sent to the FPGA." *Id.* (citing Ex. 2006 ¶ 65). Patent Owner

additionally argues that Akasaka's teachings regarding common memory data does not involve processing of data shared between a microprocessor and an FPGA. *Id.* at 32–33 (citing Ex. 1005, 11, Fig. 25(c); Ex. 2006 ¶¶ 66–67). Patent Owner additionally argues that, because the combination does not teach or suggest the processing of shared data, it also does not teach or suggest accelerating such processing. *Id.* at 34. Lastly, Patent Owner suggests that the combination does not teach or suggest limitation 1.3 of claim 1 because it does not disclose memory accessible to a microprocessor and FPGA with approximately equal speed. *Id.* at 35–36 (citing Ex. 2006 ¶ 70).

Each of these arguments is based on Patent Owner's interpretation of limitation 1.3, which we do not agree with and have addressed above, in Section II.C.4. Considering the record and arguments made, Petitioner has shown that the combination of Zavracky, Chiricescu, and Akasaka teaches both data shared between the FPGA and the microprocessor, and also how a three-dimensional approach as in Zavracky (with shorter busses), the distributed contact points and shorter interconnects of Akasaka, and the stacked arrangement of Chiricescu combine to teach or suggest accelerated processing of data shared between the microprocessor and the FPGA, for example, for reconfiguring the FPGA. *See* Pet. 28–31 (citing Ex. 1003, 3:1– 11, 6:1–12, 12:28–38; Ex. 1004, 3; Ex. 1005, 3, 11; Ex. 1002 ¶¶ 342–348).

d. Conclusion – Claim 1

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claim 1 would have been obvious.

5. *Claims 2–6*

Claim 2 depends from claim 1 and further recites that the processor module further comprises "at least one memory integrated circuit die element stacked with and electrically coupled to" either the field programmable gate array IC die element (of limitation 1.1) or the microprocessor IC die element (limitation 1.2) of claim 1. Ex. 1001, 6:27–31. Petitioner argues that Zavracky's figures 12 and 13 describe a layer including random access memory. Pet. 32 (citing Ex. 1003, 11:63–65, 12:33–35, Figs. 10, 12, 13). Petitioner further argues that this layer is, in the combination of Zavracky, Chiricescu, and Akasaka, stacked with and electrically coupled to the other die elements as explained with reference to the die elements of claim 1. *Id.* at 32–33 (citing Ex. 1003, 11:63–65, 12:15– 28, 12:33–35, Figs. 10, 12; Ex. 1004, 1; Ex. 1002 ¶ 319).

Claim 3 depends from claim 1 and further recites that "said programmable array is configurable as a processing element." Ex. 1001, 6:32–33. Petitioner argues that Zavracky's programmable array functions as a processing element. Pet. 34 (citing Ex. 1003, 12:28–38; Ex. 1002 ¶ 302). Petitioner further contends that Chiricescu's FPGA can be reconfigured as a processing element. *Id.* (citing Ex. 1004, 2, 3; Ex. 1002 ¶ 302).

Claim 4 depends from claim 1 and further recites that "at least one field programmable gate array and said at least one microprocessor integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements." Ex. 1001, 6:34–38. Claim 5 depends from claim 4 and further requires that "said

contact points traverse said die elements through a thickness thereof." Ex. 1001, 6:39–40. Claim 6 depends from claim 5 and further requires that "said contact points traverse said die elements through a thickness thereof." Ex. 1001, 6:41–43. Patent Owner argues that the limitations of claims 4 and 5 are taught by Zavracky's "openings or via holes" providing inter-layer connections placed anywhere on the die, and Akasaka's layers connected through via holes. Pet. 36–39 (citing Ex. 1003, 6:43–7, 13:43–46. 14:56–63; 1005, 2–5; Ex. 1002 ¶¶ 313–316, 327–334).

With respect to Claim 6, Petitioner argues that the general knowledge of one of ordinary skill in the art would have been that die elements are thinned to a point at which contact points traverse the thickness of the elements, and that one of ordinary skill would have known to employ this thinning, including because of Zavracky's suggestion of a need for thin stacks and contact point traversal. *Id.* at 39–41 (citing Ex. 1003, 13:54–57; Ex. 1002 ¶¶ 262–266, 335–341).

Except for arguments with respect to claim 1, addressed above, Patent Owner presents no arguments relating to these dependent claims.

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claims 2–6 would have been obvious.

E. *Obviousness, Claims 7–12*

Claim 7 largely tracks the limitations recited in claim 1, but additionally includes a limitation, 7.3, that "at least one field programmable gate array integrated circuit die element being configured to provide test stimulus to the at least one microprocessor integrated circuit die element during

manufacture and prior to completion of the module packaging." Ex. 1001, 6:44–57. Claims 8, 9, 10, 11, and 12 duplicate the additional limitations of claims 2, 3, 4, 5, 6, 7, and 8, respectively. Petitioner argues that claims 7–12 are unpatentable in view of a combination of Zavracky, Chiricescu, Akasaka, and Satoh. Pet. 41–46.

1. *Satoh*

Satoh, titled "Semiconductor Integrated Circuit, Method for Testing the Same, and Method for Manufacturing the Same," describes using an FPGA to generate test stimuli to test elements on the same chip. Ex. 1008, code (54). Satoh describes a test circuit formed in a portion of the FPGA and used to test a CPU. *See* Ex. 1008, 14, Fig. 7.

2. *Claim 7*

Petitioner proposes one of ordinary skill would have combined Satoh with Zavracky, Chiricescu, and Akasaka, to teach or suggest the requirements of limitation 7.3, with the other limitations taught as discussed with respect to claim 1. Pet. 42, 44–45 (citing Ex. 1008, 5:16–22, 7:36-8:1, 45:4–36, 47:6–14; Ex. 1002 ¶¶ 350–56). Petitioner argues that one of ordinary skill would have used Satoh's teachings with respect to using an FPGA to test circuitry to achieve known predictable benefits in testing, chip real estate, and design complexity, and would have had a reasonable expectation of success in the combination. *Id.* at 43–44 (citing Ex. 1002 ¶¶ 241–244). Petitioner argues that Satoh's teaching of an FPGA providing a test signal and an expected value signal to test a CPU teaches "at least one field programmable gate array integrated circuit die element being configured to provide test stimulus to the at least one

microprocessor integrated circuit die element during manufacturing." *Id.* at 44–45 (citing Ex. 1008, 3:5–8, 5:16–22, 7:36-8:1, 45:4–36, 46:4–36, 47:6–14; Ex. 1002 ¶¶ 350–356). Petitioner further contends that one of ordinary skill would have understood this to occur "prior to completion of the module packaging," because Satoh teaches the testing occurs to ensure high yield, and one of ordinary skill would have recognized that testing prior to packaging would avoid the expense and waste of packaging a module that would not be part of the hoped-for yield. *Id.* at 45 (citing Ex. 1008, 2:32–35, 3:22–23; Ex. 1043 ("Mess"); Ex. 1002 ¶¶ 355–356); Pet. Reply 16–17 (citing Ex. 1009; Ex. 1020; Ex. 1043 ¶ 37; Ex. 1002 ¶ 241).

Patent Owner argues that Satoh does not teach or suggest an FPGA used to test the CPU prior to completion of the module packaging. PO Resp. 45–46. Patent Owner contends that Satoh's teaching is that testing could improve yield by detecting defective parts of the FPGA and avoiding those parts. *Id.* (citing Ex. 1008, 4–5; Ex. 2006 ¶ 83). Dr. Souri testifies that this teaching of Satoh "demonstrates that Satoh describes a process of improving yield by avoiding defective parts of an FPGA when using the FPGA to test other internal circuits, not by ensuring that the testing is conducted 'prior to packaging being finished,' as asserted in the Petition." Ex. 2006 ¶ 83. Thus, Dr. Souri testifies, Satoh teaches a technique to improve yield for integrated circuit dies even if portions of dies are defective. *Id.* ¶ 84.

Patent Owner argues that Satoh does not teach testing a stacked microprocessor, and that this is why Petitioner relies on Mess. PO Resp. 47. Patent Owner contends that Mess, cited by Petitioner, describes

testing individual dies prior to stacking. PO Resp. 47–49 (citing Ex. 1043 ¶¶ 6, 36, 38; Ex. 2006 ¶¶ 86–87); PO Sur-reply 16. Patent Owner argues that, while another embodiment of Mess teaches that a stacked die package that passes testing optionally may be encapsulated, because Mess describes the encapsulating layer is optional and the only step left after testing the stacked die package, Mess does not support Petitioner's arguments with respect to limitation 7.3. PO Resp. 48–49 (citing Ex. 1043 ¶ 46, Fig. 8; Ex. 2006 ¶ 88).

We agree with Petitioner that these arguments do not address the combined teaching of the asserted references, with respect to what one would understand about testing the stacked die package taught by Zavracky, Chiricescu, and Akasaka. Pet. Reply 14. Thus, Patent Owner's argument that Petitioner must rely on Mess to bolster the contentions regarding the teachings of Satoh is rendered moot. Furthermore, given Patent Owner's acknowledgment that Mess teaches a stacked die package being encapsulated only if it passes testing, we agree with Petitioner that this shows, as Petitioner argues, that one of ordinary skill would have recognized that this testing should occur before packaging. *See* Pet. 45. While the encapsulation is optional, Mess teaches that it occurs (if it occurs) only if the stacked die package passes testing. Ex. 1043 ¶ 46; Ex. 2006 ¶ 8. Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claim 7 would have been obvious.

3. *Claims 8–12*

Claims 8–12 are argued by Petitioner with respect to the arguments relating to claim 7 and

claims 2–6. Pet. 45–46. Patent Owner presents no additional arguments relating to these dependent claims. For the same reasons given with respect to those claims, Petitioner persuasively shows that claims 8–12 would have been obvious.

F. *Obviousness, Claims 13–30*

Petitioner contends claims 13–30 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. *See* Pet. 46–62. Patent Owner contests the showing with respect to limitations and 22.4, and with respect to the combination of art proposed by Patent Owner. PO Resp. 52–73; PO Sur-reply 17–26.

1. *Trimberger*

Trimberger, titled "A Time-Multiplexed FPGA" (1997), teaches an FPGA with on-chip memory distributed around the chip. Ex. 1006, 1. Trimberger teaches that the memory "can also be read and written by on- chip [FPGA] logic, giving applications access to a single large block of RAM." *Id.* Trimberger teaches that "the entire configuration of the FPGA can be changed in a single cycle of the memory" and that "[w]hen the device is *flash reconfigured*, all bits in the logic and interconnect array are updated simultaneously from one memory plane." *Id.* Trimberger teaches 100,000 bit lines that may be involved in reconfiguration. *Id.* at 27.

2. *Claim 13*

Petitioner contends claims 13 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. *See* Pet. 47–57.

With the exception of limitation 13.4, the Petition relies on the teachings or suggestions of Zavracky, Chiricescu, and Akasaka to teach or suggest the limitations of claim 13, as described with respect to claim 1 or claim 2. Pet. 50–51. We have addressed these in Sections II.D.4 and II.D.5. With respect to limitation 13.4, "means for reconfiguring the programmable array within one clock cycle," we have concluded that the corresponding structure is "a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element." *See supra* § II.C.2. We have additionally concluded that a wide configuration port should be construed as "a configuration data port connecting in parallel cells on one die element to cells on another die element." *See supra* § II.C.1.

a. Petitioner's Showing

Our constructions correspond most closely to Petitioner's arguments with respect to the second structure it proposed for means-plus-function limitation 13.4, "a stacked FPGA die and memory die interconnected by a wide configuration data port using contact points distributed throughout the dies." *See* Pet. 11–13. Petitioner contends that the combination of Zavracky, Chiricescu, Akasaka, and Trimberger teaches or suggests this second structure, including in the die elements connected by contact points distributed throughout the dies. Pet. 56–57 (referencing *id.* at 35–37). Petitioner argues that Akasaka describes that its active layers are interconnected through "several thousands or tens of thousands of via holes" distributed throughout the surfaces of the die elements. *Id.* at 36–37 (citing Ex.

1005, 3, 5; Ex. 1002 ¶¶ 327–332). Petitioner additionally presents Dr. Franzon's declaration to the effect that this configuration was "ubiquitous" in the prior art. *Id.* at 37 (citing Ex. 1020, Fig. 4; Ex. 1021, Fig. 1(a); Ex. 1028, Fig. 2(b); Ex. 1002 ¶ 332). Petitioner argues that these interconnections and Trimberger's memory access port teach or suggest the wide configuration data port. *Id.* at 56–57. Petitioner references its discussion of Trimberger with reference to its first proposed structure for 13.4, in which Petitioner argues that Trimberger includes a wide configuration data port in the single access memory access port that "has a direct connection to each of the buffer memory cells around the chip" using "massive connectivity within the chip." *Id.* at 51–54 (citing Ex. 1006, 22, 26, 27; Ex. 1002 ¶ 367).

Petitioner argues that one of ordinary skill would have combined Trimberger with Zavracky, Chiricescu, and Akasaka to obtain the benefits of the one-cycle FPGA reconfiguration of Trimberger. Pet. 48–49. Petitioner argues that the motivation would have been to address Chiricescu's stated issue with high configuration time for an FPGA; to prevent data from being dropped during reconfiguration; and to address the delays arising from a shared bus as in Zavracky. *Id.* at 48–49 (citing Ex. 1004, 1; Ex. 1003, 5:55– 56; Ex. 1002 ¶¶ 252–254). Petitioner further argues that one of ordinary skill would have expected success in using a memory and area-wide interconnections as in Trimberger for reprogramming an FPGA in one clock cycle, given the state of the art at the time of the invention. *Id.* at 49 (citing Ex. 1020; Ex. 1021; Ex. 1041; Ex. 1047; Ex. 1002 ¶ 256).

b. Patent Owner's Contentions and Our Analysis

Patent Owner contends that the Petition mapped Trimberger's "single memory access port" to the wide configuration data port, and that the single memory access port is a narrow port. PO Resp. 53–54; PO Sur-reply 17–19. Patent Owner additionally contends that Petitioner has impermissibly shifted its theory in its Reply. PO Sur-reply 18–19. Patent Owner additionally contends that the Petition's contentions are deficient because they involve the single memory access port of Trimberger which, Patent Owner argues, is not involved in the reconfiguration of the FPGA. PO Resp. 55–58 (citing Ex. 2006 ¶¶ 96–101). Thus, Patent Owner argues, Petitioner has improperly relied on the functionality from one portion of Trimberger (one-cycle reconfiguration) and the structure from another portion of Trimberger (memory access port). *Id*.

While our final constructions are not identical to those in the Decision on Institution, here and in that Decision we focused on the second corresponding structure proposed by Petitioner, and in Petitioner's arguments relating to that, Petitioner contends that

> [t]he wide configuration data port (i.e., the place through which the configuration data is transferred to each of the configuration logic cells in the FPGA) using the contact points, is provided by Zavracky in combination with Chiricescu and Akasaka (and in particular, the "thousands or several tens of thousands of via holes are present in these devices" taught by Akasaka), and Trimberger (for the "memory access port" that connects to the configuration data "memory

> plane"). As discussed, integration of Trimberger's teachings yields the claimed function of "reconfiguring the programmable array within one clock cycle."

Pet. 56–57. We consider this argument, which was clearly stated in the Petition, and find it persuasive. Patent Owner's arguments relate to constructions including buffer cells, which we have not adopted, or to the teachings of Trimberger in isolation, rather than in combination with the teachings of the art in combination. The Petition persuasively shows that limitation 13.4 is taught, not by Trimberger's teachings regarding the "single memory access port" that provides access to configuration memory (Pet. 51, 57; Ex. 1006, 26) alone, but rather in combination with the description in Trimberger of instantly switching to a new configuration with bit lines for a memory plane read simultaneously from configuration memory (Pet. 53–55; Ex. 1006, 27) and with Akasaka's teaching of thousands or tens of thousands of via holes (Pet. 56–57; Ex. 1005, 3, 5). This argument, which after considering the record we find persuasive, was present in the Petition. We agree with Petitioner that the combination of Zavracky, Chiricescu, and Akasaka with Trimberger yields a structure corresponding to the claimed tructure (a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element) and the function of reconfiguring the programmable array within one clock cycle.

We recognize Patent Owner's argument that "a petitioner cannot rely on one reference for the structure and turn to another reference for the

function to demonstrate that the prior art is present in both the function and corresponding structure." PO Sur-reply 20–21 (citing *Fresenius USA, Inc. v. Baxter Int'l, Inc.*, 582 F.3d 1288, 1299 (Fed. Cir. 2009); *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1361 (Fed. Cir. 2001) (Michel, J. dissenting)). The relevant portion of *Fresenius* involved a dispute regarding whether claims with means-plus-function limitations were shown to be invalid. *Fresenius*, 582 F.3d at 1293–94. Our reviewing court found that there was no evidence of what the correct corresponding structure was for certain means-plus-function limitations, and no comparison of structure in the specification to those present in the prior art. *Id.* at 1299–1300. While the Federal Circuit took the opportunity to stress that, for showing invalidity of a claim with a means-plus-function limitation, both the function and the corresponding structure must be found to be present in the prior art, we do not see any indication in this case relating to Patent Owner's assertion of impropriety in finding structure and function in an asserted combination based on the combined teachings of references. And Judge Michel, in the *McGinley* dissent, was discussing a single-reference obviousness analysis, thus structure and function would necessarily be in the same reference, and no inference can be made regarding Judge Michel's opinion regarding invalidity arguments for means-plus-function claims based on a combination of multiple references. *See McGinley*, 262 F.3d at 1361.

Patent Owner argues that Petitioner "rel[ies] on one reference for the structure and turn[s] to another reference for the function." PO Sur-reply 20. But this is not the case here. Rather, Petitioner presents the structure in a combination of Zavracky, Chiricescu,

Akasaka, and Trimberger and the function from relevant portions of Trimberger, with specific reference to the function attributed by Trimberger to the structure included from Trimberger in the asserted combination. We find no error in such an analysis.

Patent Owner also argues that the references do not teach buffer cells, and that Trimberger's configuration memory would not correspond to buffer cells as the data is not transiently stored in configuration memory. PO Resp. 59–64. These arguments are moot in view of our constructions, which do not require buffer cells.

Lastly, Patent Owner argues that one of ordinary skill in the art would not have been motivated to combine Zavracky, Chiricescu, Akasaka, and Trimberger. First, Patent Owner reiterates the contentions previously addressed with respect to the combination of Zavracky, Chiricescu, and Akasaka relating to claim 1. PO Resp. 65–66. Patent Owner also argues that, because Trimberger provides on-chip memory, a combination with Zavracky, Chiricescu, and Akasaka would require a change in that combination, with the memory no longer stacked in a separate die with the FPGA and microprocessor dies. *Id.* at 67–69. Patent Owner additionally argues that because of the requirement that Trimberger's configuration memory must be on the same chip as the FPGA, one of ordinary skill would not have been motivated to or capable of making the combination. These arguments, however, do not consider what the combination of the art would have suggested to one of ordinary skill or relate to the proposed combination, in which a memory die would be used in place of the

on-chip memory of Trimberger. Pet. 47–49, 56–57; *see* Pet. Reply 28. No evidence or rationale cited by Patent Owner shows that the location of Trimberger's on-chip memory is necessary in some way to Trimberger's teachings. As detailed above, Petitioner presents a discussion of the use of a separate memory plane and a wide configuration data port and describes the motivation that one of ordinary skill would have had for the combination of Trimberger's teachings with those of Zavracky, Chiricescu, and Akasaka. Pet. 48–49.

c. Conclusion – Claim 13

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claim 13 would have been obvious.

3. *Claims 14–21*

Claims 14–21 are argued by Petitioner largely with respect to the arguments relating to claims 1, 4–7, and 13. Pet. 57–60. Patent Owner presents no additional arguments relating to these dependent claims. For the same reasons given with respect to those claims, Petitioner persuasively shows that claims 14–21 would have been obvious.

4. *Claims 22–30*

Claim 22 is argued by Petitioner with respect to the arguments made relating to claim 13, with the exception of limitation 22.1's inclusion of "a plurality of configuration logic cells" on the integrated circuit die element that includes a programmable array. For this limitation, Petitioner contends that Trimberger describes an FPGA with a plurality of configurable logic block configuration cells. Pet. 60–61 (citing Ex. 1006, 26; Ex. 1044; Ex. 1002 ¶¶ 300–301).

Claims 23–30 are argued with respect to arguments presented for claims 6, 14, 15, 16, 17, 18, 19, 20, and 22. Pet. 61–62.

Patent Owner presents no additional arguments relating to claim 22 or dependent claims 23–30.

For the same reasons given with respect to those claims, Petitioner persuasively shows that claims 22–30 would have been obvious.

G. *Exhibit 1070*

Patent Owner argues that "[p]aragraphs 5–9, 23–28, 42–56, 59–65, 73–74, 76–77, 95–105, and 110–118 from Dr. Franzon's [Reply D]eclaration (Ex. 1070) addressing Petitioner's alleged obviousness grounds are not sufficiently discussed in the Reply" at pages 13, 22, and 27–29 of the Reply. Sur-reply 27. Patent Owner contends that the noted paragraphs are "not discussed in the Reply, but instead incorporated by citation or a cursorily parenthetical." *Id.* Patent Owner further contends that "the Board should not and cannot play archeologist with the record to search for the arguments" and "should not . . . consider[] Dr. Franzon's arguments." *Id.* (citing 37 C.F.R. § 42.6(a)(3) ("Arguments must not be incorporated by reference from one document into another document.").

Patent Owner also cites *Gen. Access Sols., Ltd. v. Sprint Spectrum L.P.*, 811 F. App'x 654, 658 (Fed. Cir. 2020) as "upholding the Board's finding of improper incorporation by reference because, *inter alia*" (Sur-reply 25), "'playing archaeologist with the record' is precisely what the rule against incorporation by references was intended to prevent," (*id.* (quoting *Gen. Access Sols.*, 811 F. App'x at 658, internal citation

omitted)). The situation here is different than in the cited case in which the court noted a problem with identifying a party's substantive arguments *prior to turning to the declaration at issue*: "*To identify GAS's substantive arguments*, the Board was forced to turn to a declaration by Struhsaker, *and further to delve into a twenty-nine-page claim chart attached as an exhibit*." *Id.* (emphasis added).

Here, Patent Owner does not describe or allege any problem with identifying Petitioner's substantive arguments. In context, the paragraphs of Dr. Franzon's Reply Declaration (Ex. 1070) cited by Petitioner properly support Petitioner's substantive arguments at the pages of the Reply identified by Patent Owner.

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.[11] In summary:

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[11] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent-able
1–6	103	Zavracky, Chiricescu, Akasaka	1–6	

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent-able	Claims Not shown Unpatent-able
7–12	103	Zavracky, Chiricescu, Akasaka, Satoh	7–12	
13–30	103	Zavracky, Chiricescu, Akasaka, Trimberger	13–30	
Overall Outcome			1–30	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–30 of the '226 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.